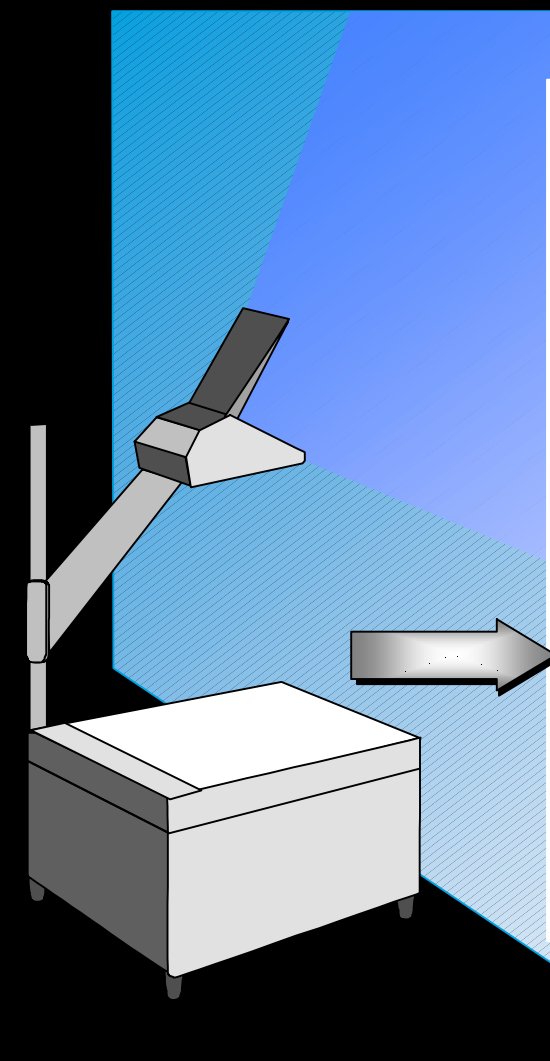


Agenda

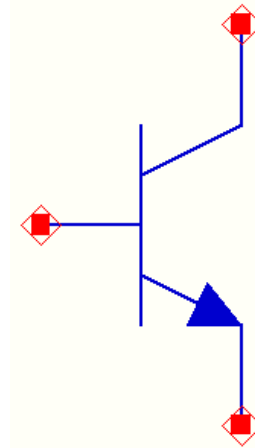
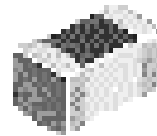
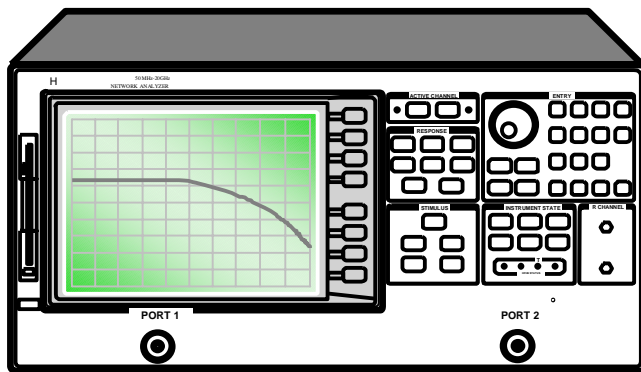


The illustration shows a measurement setup. On the left, a probe is mounted on a stand, with its tip pointing towards a device under test (DUT) on the right. A large arrow points from the DUT towards the agenda list on the right. The background is a light blue gradient.

- **Overview of RF Design Process**
- **Case study: RF Front-end**
 - + Low-noise amplifier (LNA)
 - + Duplexer
 - + Power amplifier
- **Measurement for Design**
 - + Passive Device Characterization
 - + Active Device Modeling
- **Summary**

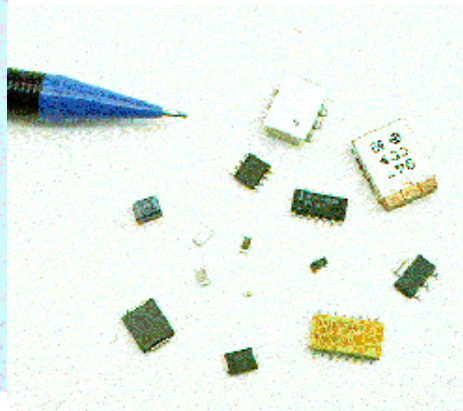
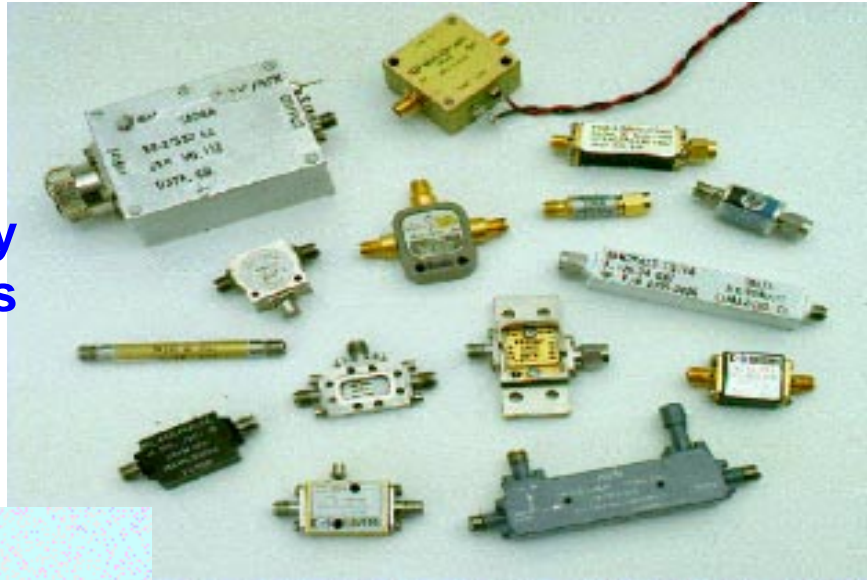
Need for Measurements During Design

- ***Measure critical components to improve models***
 - ↳ when library parts don't exist
 - ↳ when library parts were measured under different conditions (e.g. shunt vs. series)
 - ↳ if unsure of measurement conditions of library parts



RF Design: Old and New

Traditionally, RF systems used many connectorized parts



Modern designs are highly integrated and use SMT parts with a large variety of package styles and sizes

Ideal versus Real World Fixture

Ideal fixture:

- **provides transparent connection**

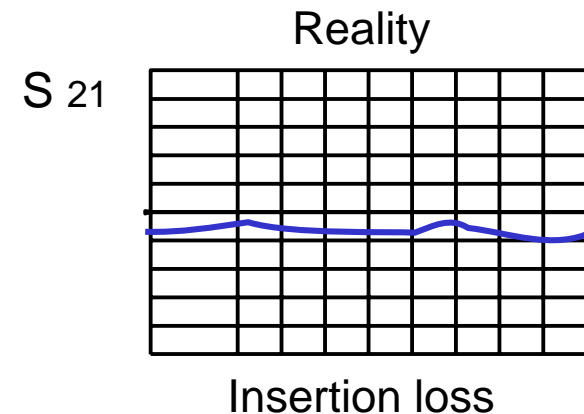
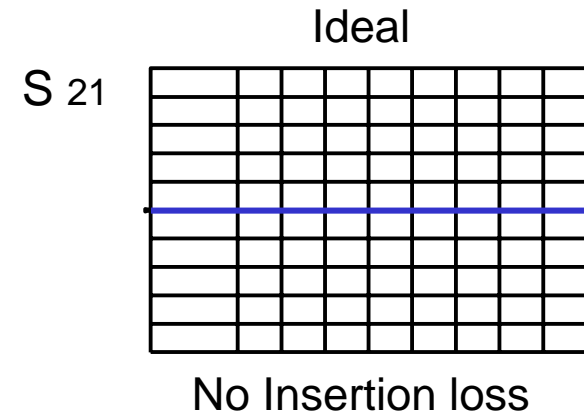
- no loss
- flat magnitude, linear phase
- no mismatches
- known electrical length
- infinite isolation

- **uses simple calibration**

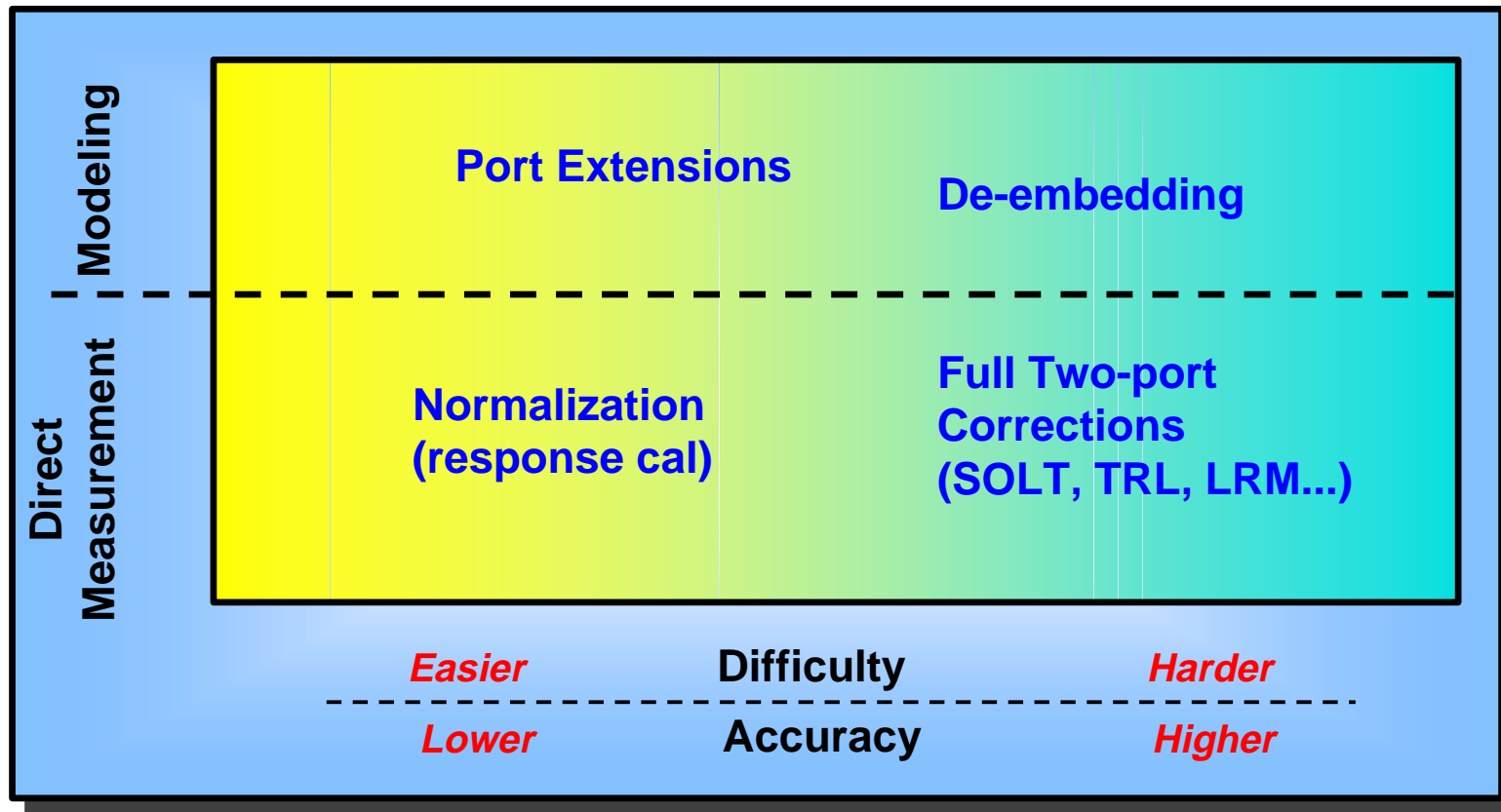
- two-port cal at end of cables
- port extensions for fixture

In the real world:

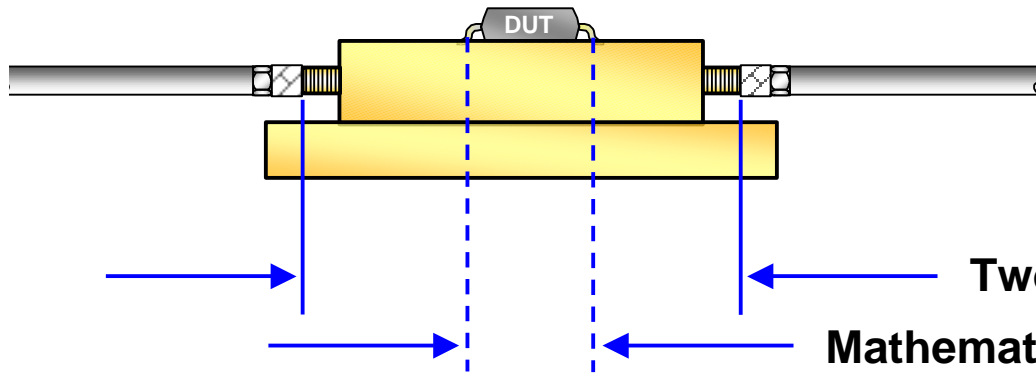
- fixture optimized relative to DUT
- calibration type depends on how well we approximate ideal fixture
- typically need calibration standards



Error-Correction Model



Modeling



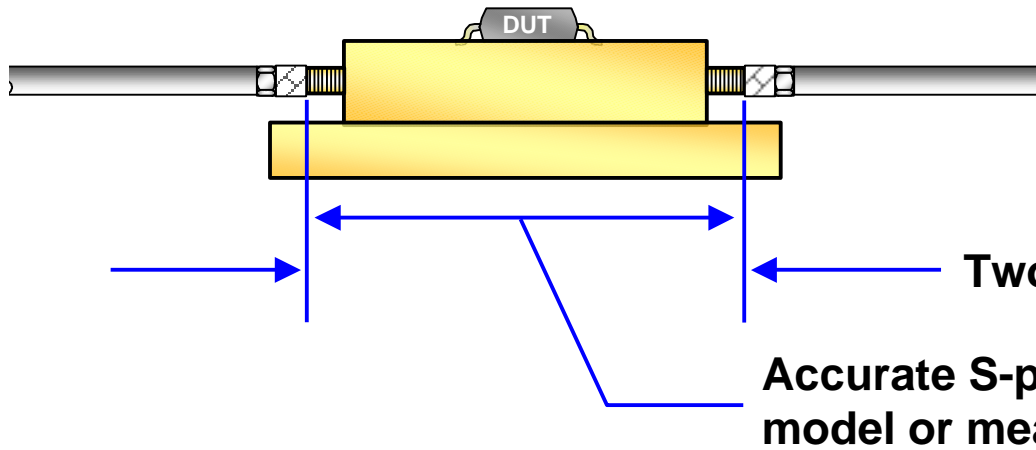
Port extensions

assume:

- no loss
- flat magnitude
- linear phase
- constant impedance

Two-port calibration reference plane

Mathematically extended reference plane



De-embedding

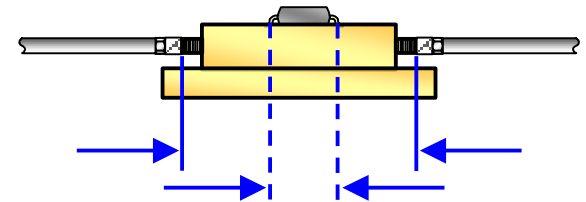
external software required

Two-port calibration

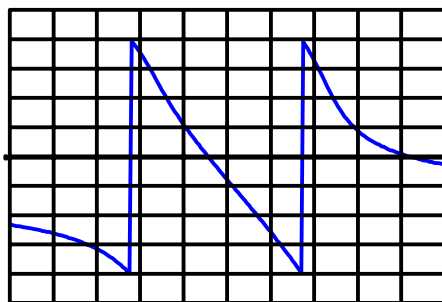
Accurate S-parameter data (from model or measurement)

Port Extensions

- port-extension feature of network analyzer removes linear portion of phase response
- accounts for added electrical length of fixture
- doesn't correct for loss or mismatch
- mismatch can occur from
 - launches
 - variations in transmission line impedance

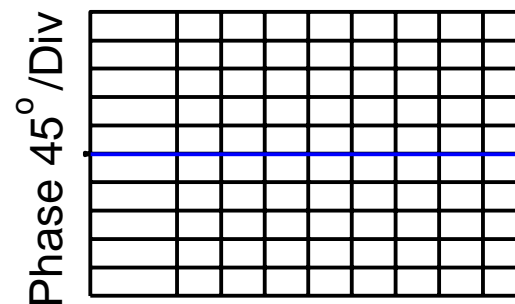


Fixture response without port extensions



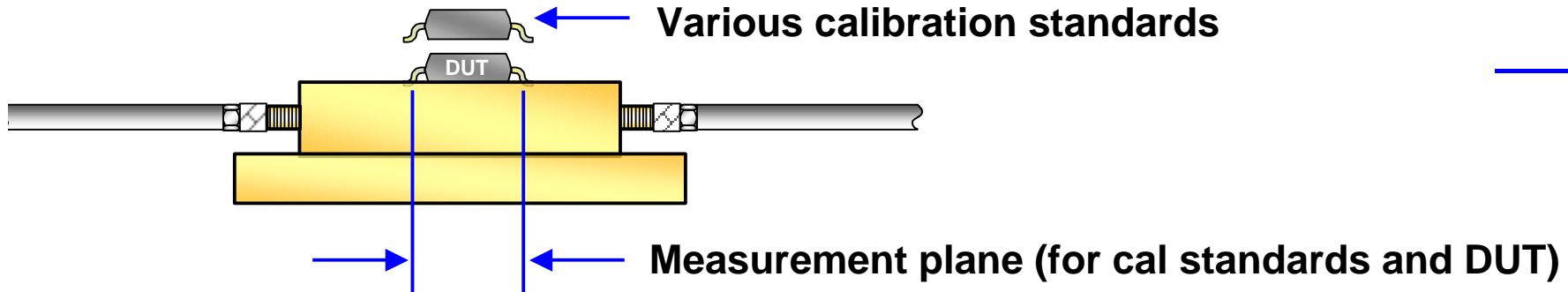
Frequency

After port extensions applied, fixture phase response is flat

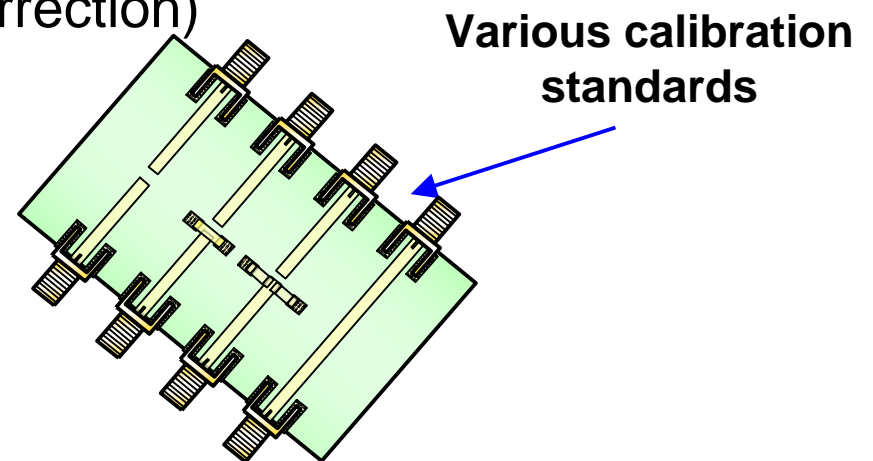


Frequency

Direct Measurement



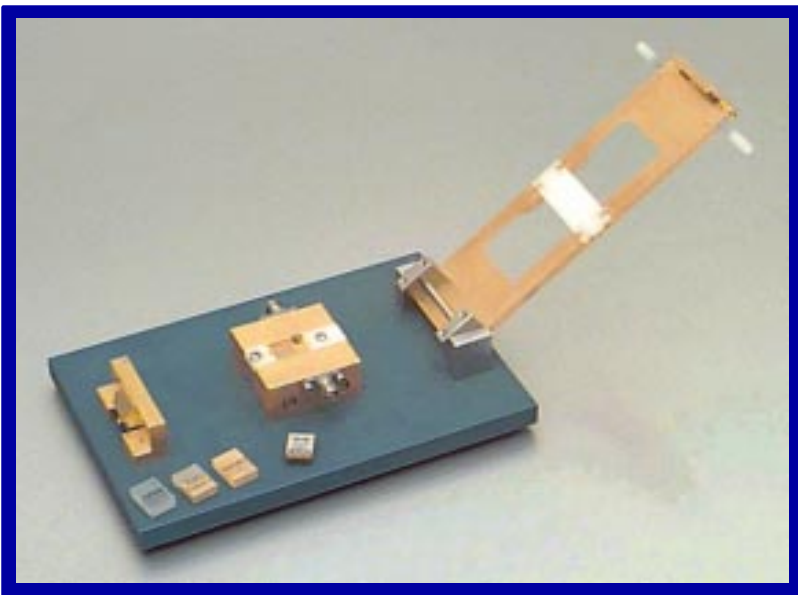
- measure standards to determine systematic errors
- two major types of calibrations:
 - response (normalization) calibration
 - two-port calibration (vector-error correction)
 - ➔ short-open-load-thru (SOLT)
 - ➔ thru-reflect-line (TRL)



Fixturing in R&D vs. Manufacturing

Manufacturing

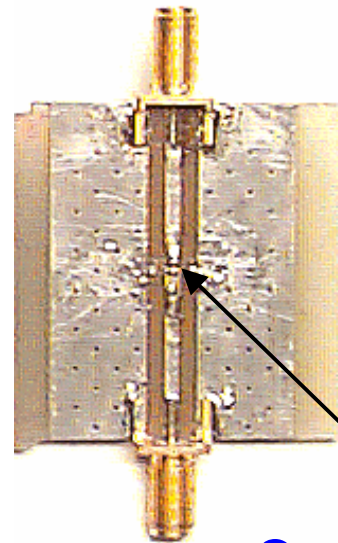
- quick insertion, alignment, clamping
- rugged for high-volume use
- compliant contacts
- usually mechanically sophisticated



Typical fixture and calibration standards for SMT manufacturing test (example: 900 MHz filter)

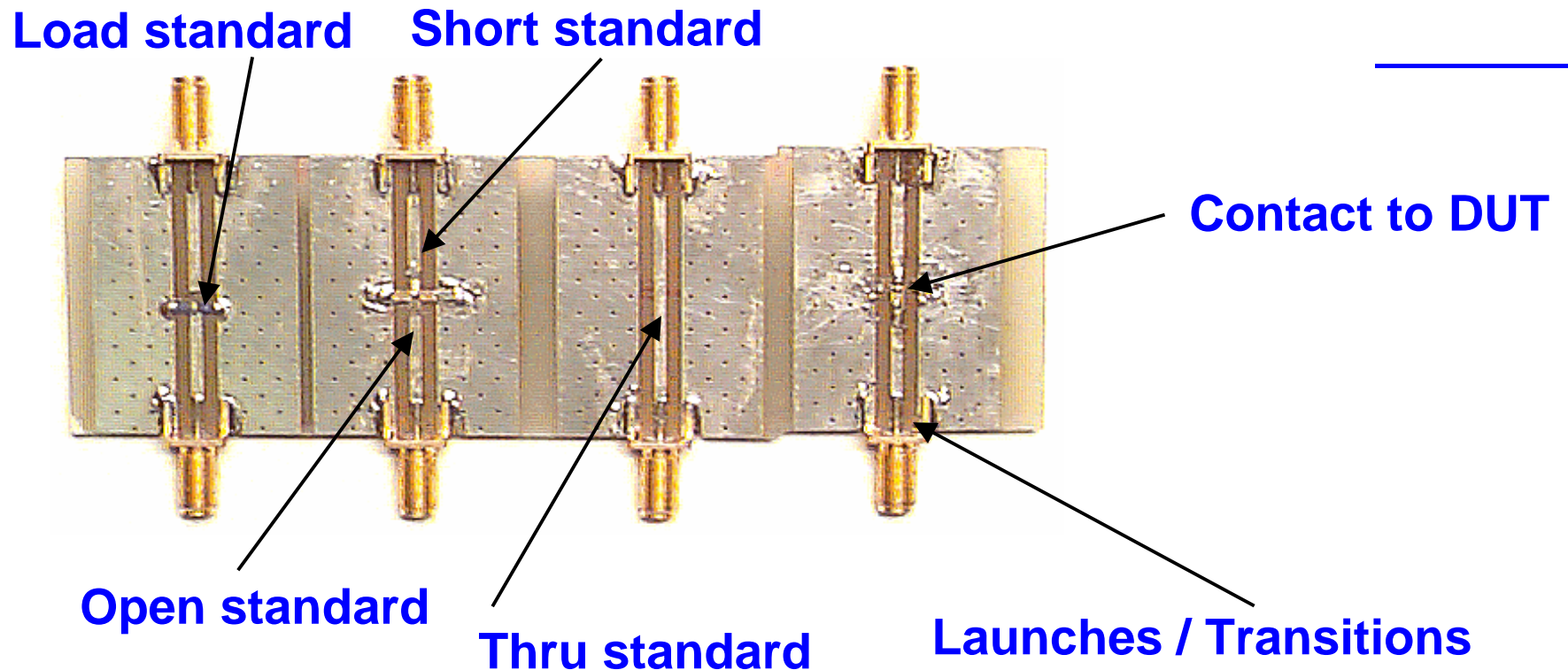
R&D

- solder parts on to fixture
- ruggedness not an issue for low volumes
- soldering handles leaded / leadless parts
- often simple (e.g., PCB with connectors)



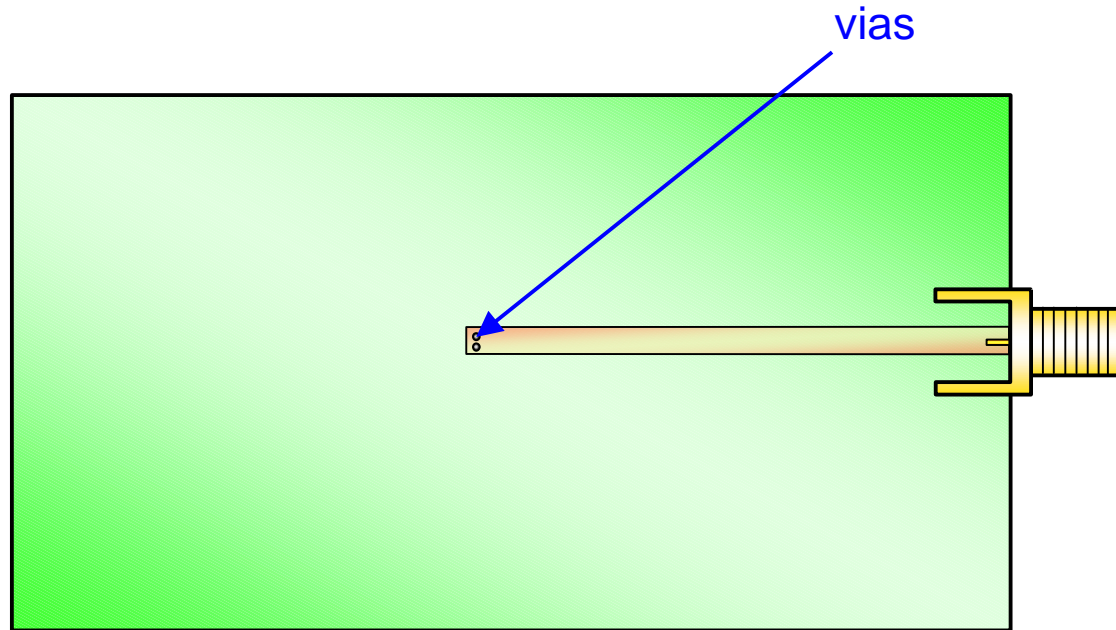
Contact to DUT

R&D Fixture with Cal Standards



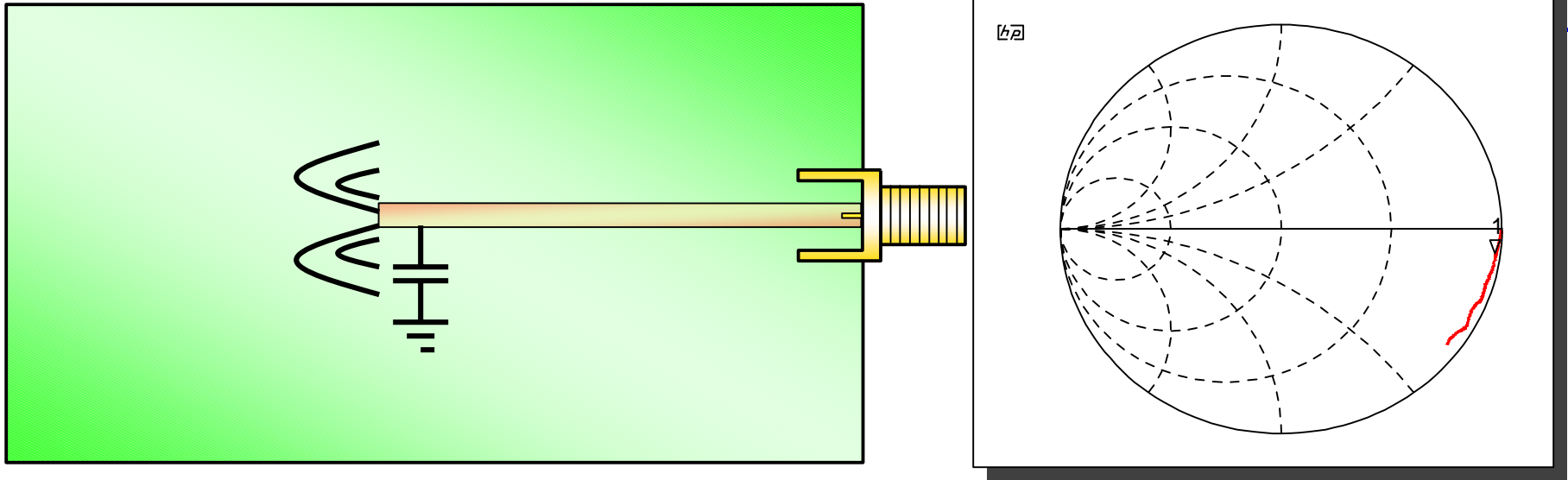
- short, thru are **easiest**
- open requires **characterization**
- load is most difficult (quality determines corrected directivity)

Short Standard



- ideal: **unity** reflection with 180° phase shift
- simply **short** signal conductor to ground (e.g. vias or metal bar)
- if using coplanar lines, short to **both** ground planes
- avoid **excess** inductance by keeping length short

Open Standard

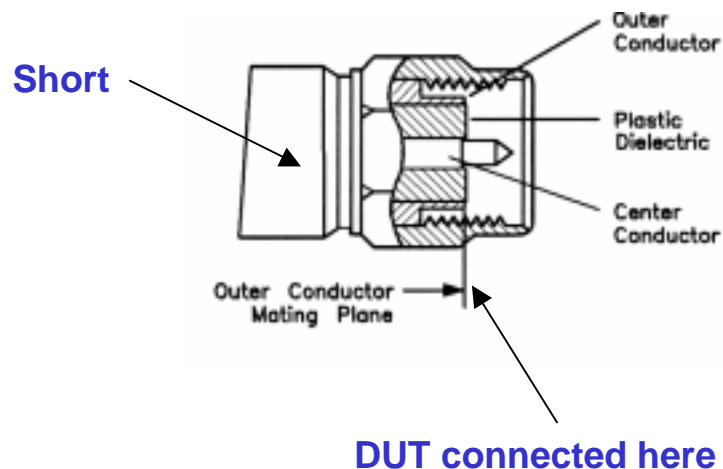


- can be **unterminated** transmission line
- ideal: unity reflection with **no** phase shift
- actual model accounts for **fringing** capacitance
(a concern around 300 MHz and above)

Calibration Kit Definition File

Calibration standards are defined in calibration kit definition file

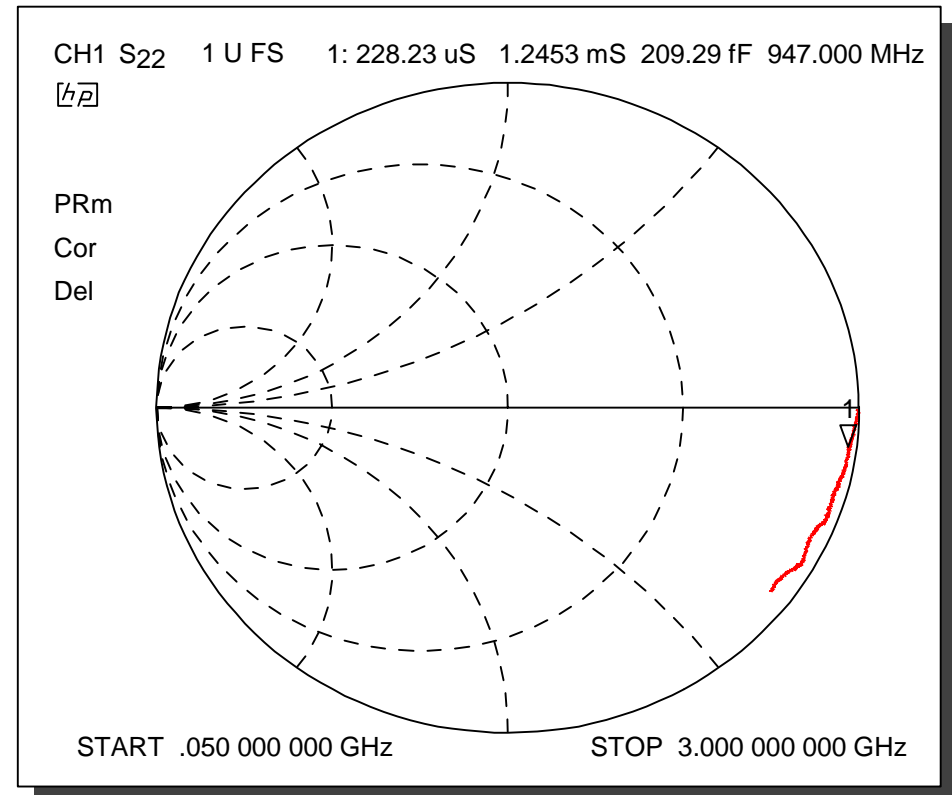
- Network analyzer contains standard (coaxial) cal-kit definitions
- Custom standards (e.g. those used with fixtures), require user to characterize and enter definitions for standards
- Cal-kit definition must match actual standards for accurate measurements



	<i>Open</i>	Short	<i>Load</i>	<i>Thru/Line</i>
Capacitance	<input checked="" type="checkbox"/>			
Inductance		<input checked="" type="checkbox"/>		
Offset delay	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Offset Zo	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Offset loss	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Min/max frequency	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Coax/waveguide	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Fixed/sliding/offset			<input checked="" type="checkbox"/>	

Determining Open Capacitance

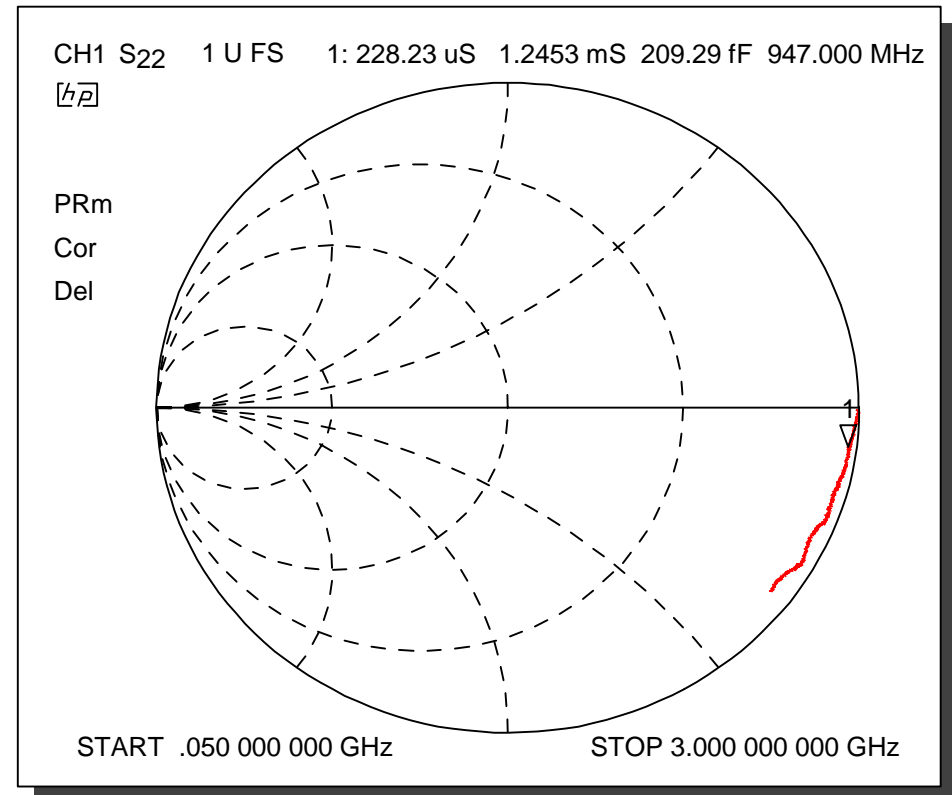
- **perform one-port calibration** at end of test cable
- **measure load**, store data in memory, display data-mem
- **measure short**, add port extension until flat 180° phase
- **measure open**, read capacitance from admittance Smith chart
- **enter capacitance** coefficient(s) in cal kit definition of open



- watch out for "negative" capacitance (due to long or inductive short)
 - ↳ adjust with negative offset delay in open <or>
 - ↳ positive offset delay in short

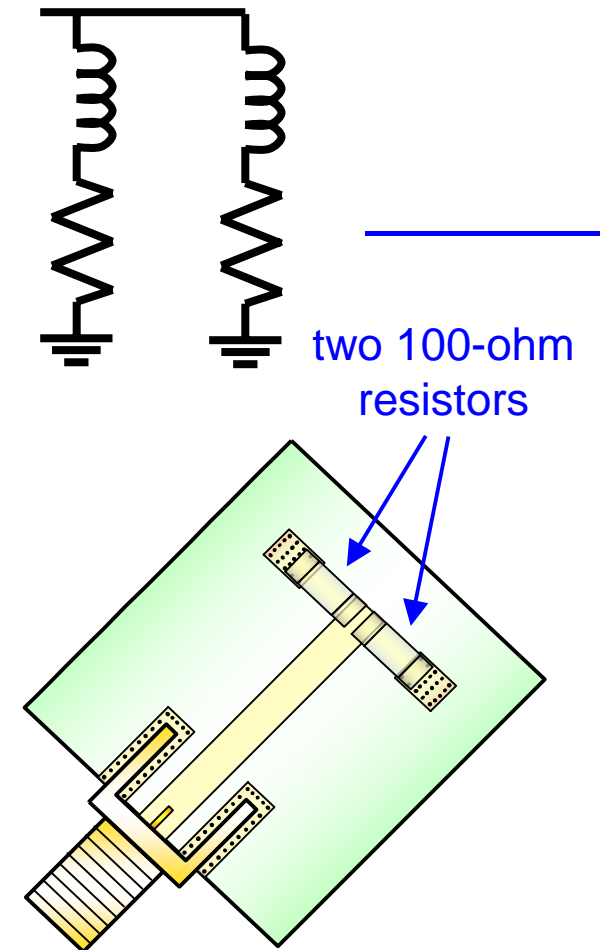
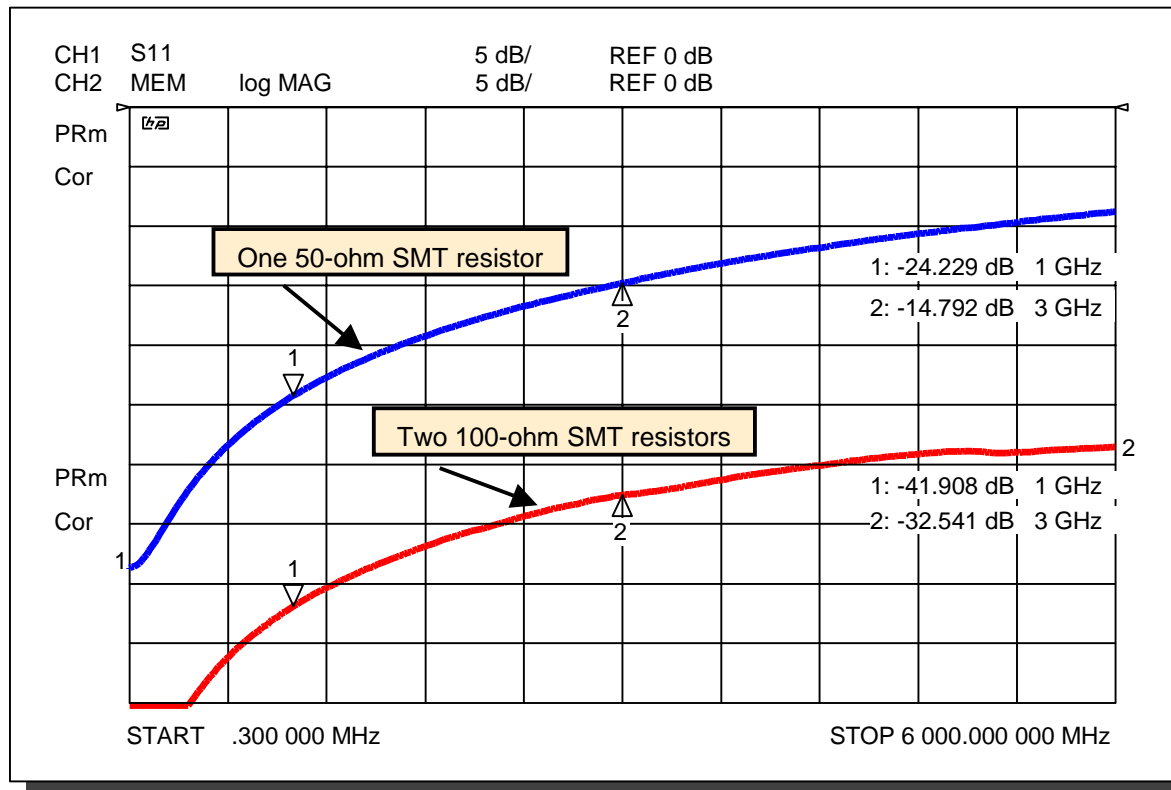
Determining Open Capacitance

- **perform one-port calibration** at end of test cable
- **measure load**, store data in memory, display data-mem
- **measure short**, add port extension until flat 180° phase
- **measure open**, read capacitance from admittance Smith chart
- **enter capacitance** coefficient(s) in cal-kit definition of open



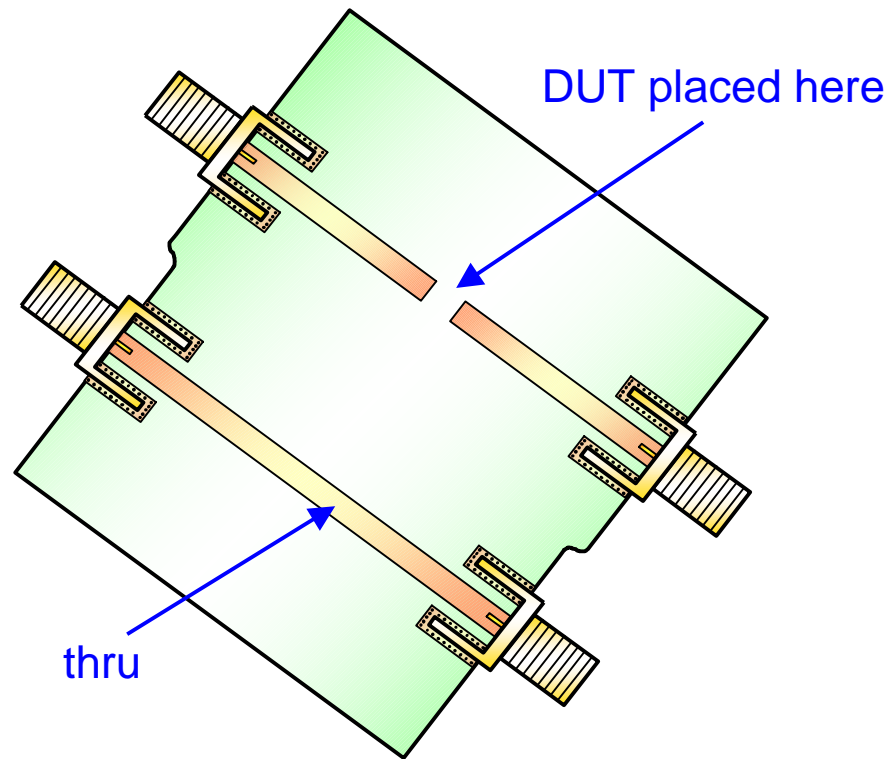
- watch out for "negative" capacitance (due to long or inductive short)
 - ↳ adjust with negative offset-delay in open *<or>*
 - ↳ positive offset-delay in short

Load Standard



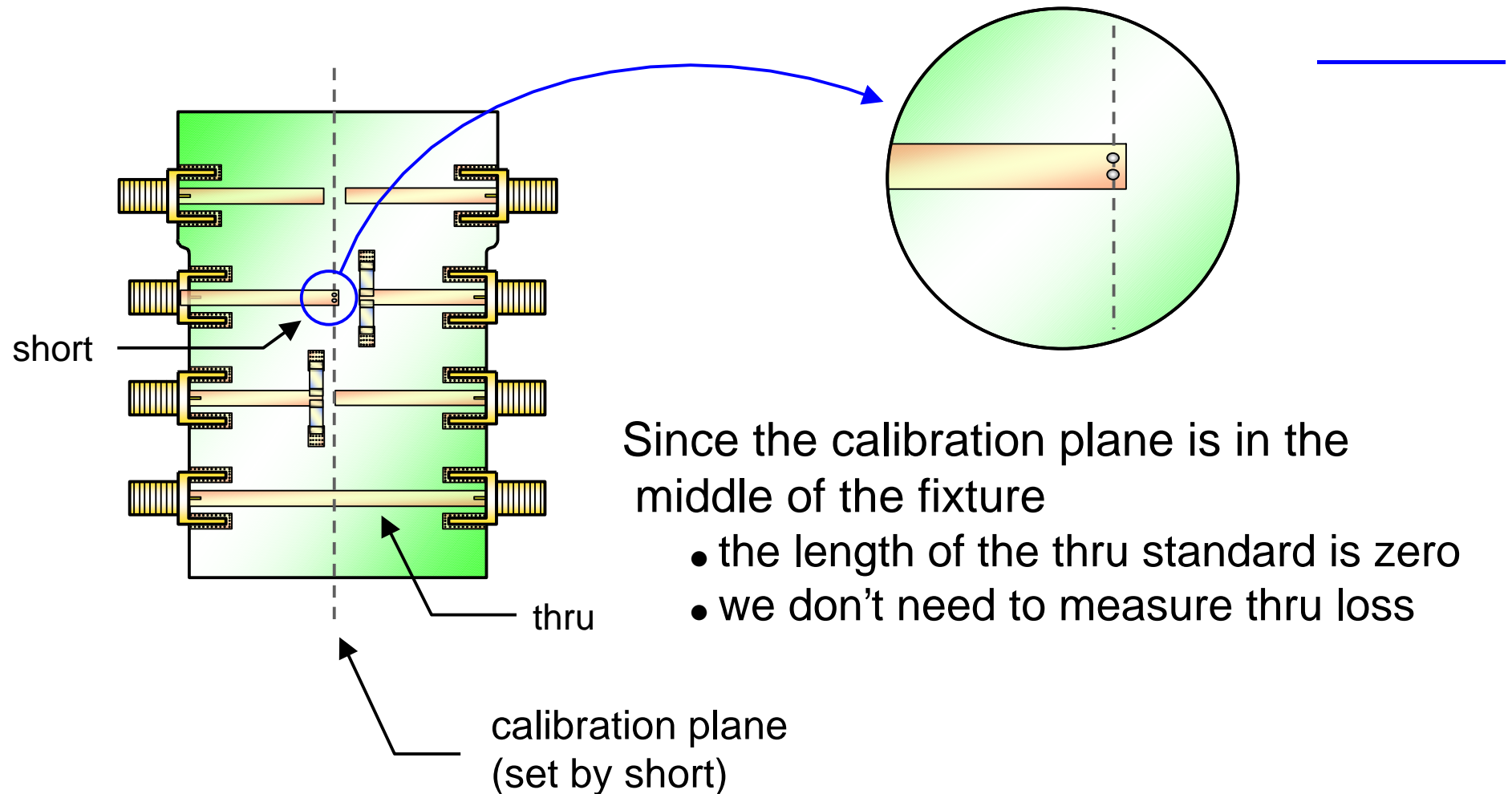
- ideal: zero reflection at **all** frequencies
- can only **approximate** at best (usually somewhat inductive)
- **two** 100-ohm resistors in parallel better than a single 50-ohm resistor

Thru Standard



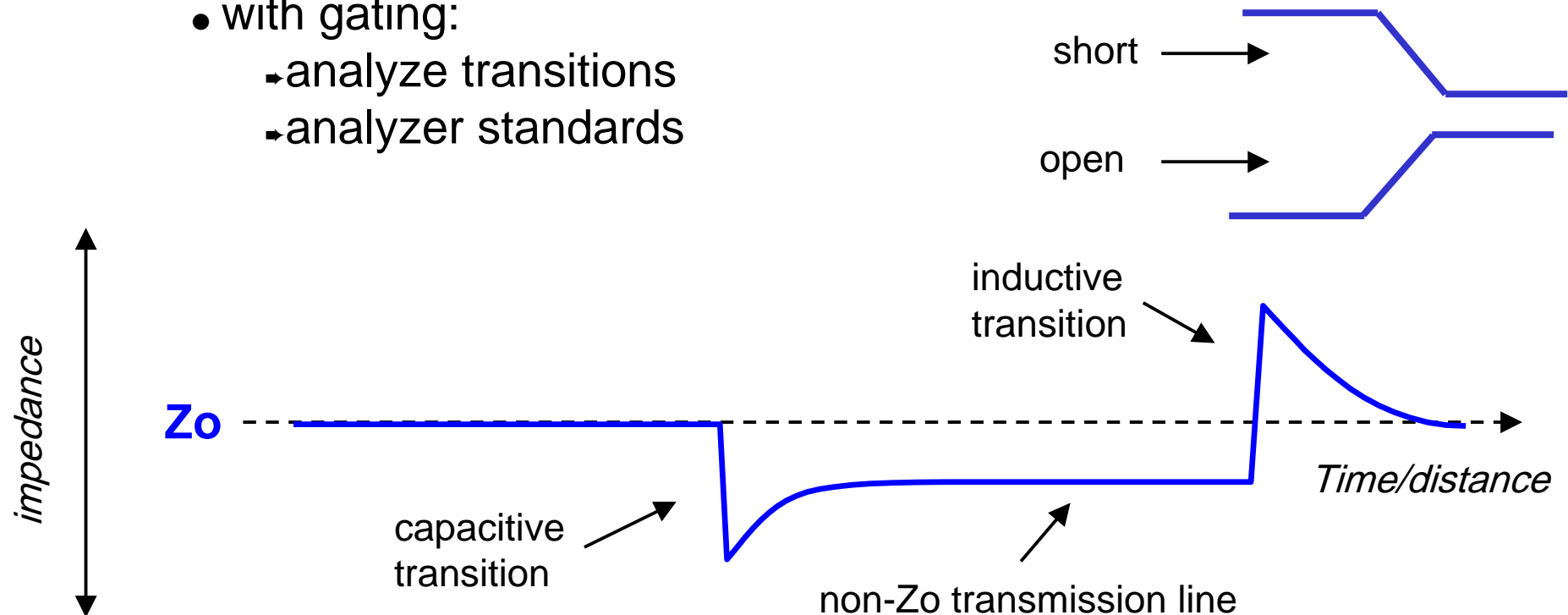
- thru is a simple **transmission line**
- desire **constant impedance** and **minimal mismatch** at ends

Characterizing Thru Standard



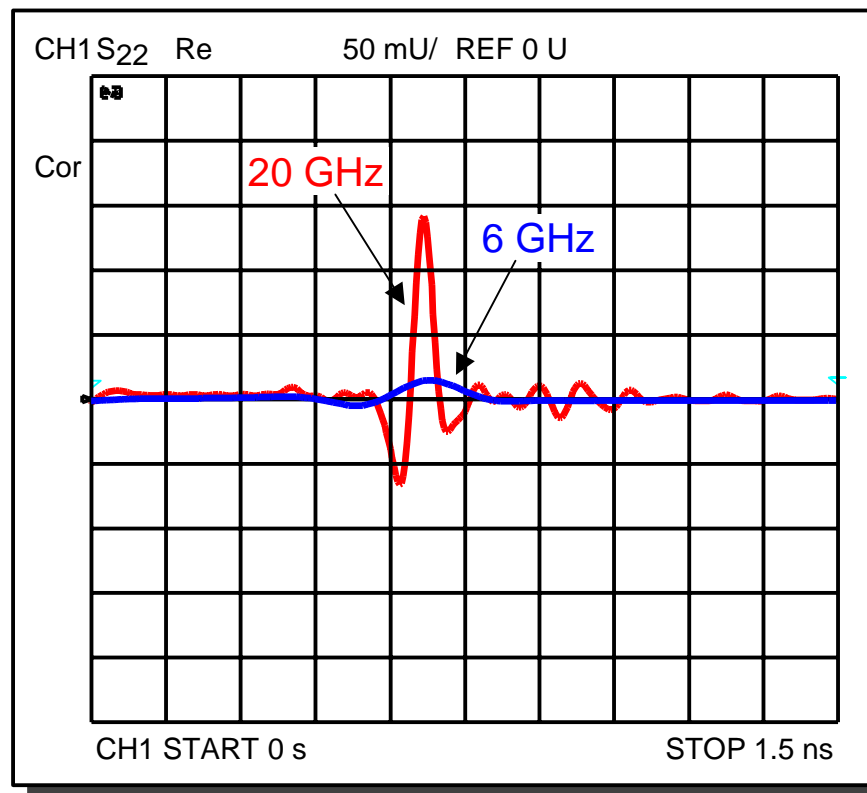
Using TDR to Evaluate Fixture and Standards

- what is TDR?
 - time-domain reflectometry
 - analyze impedance versus time
 - distinguish between inductive and capacitive transitions
- with gating:
 - analyze transitions
 - analyzer standards

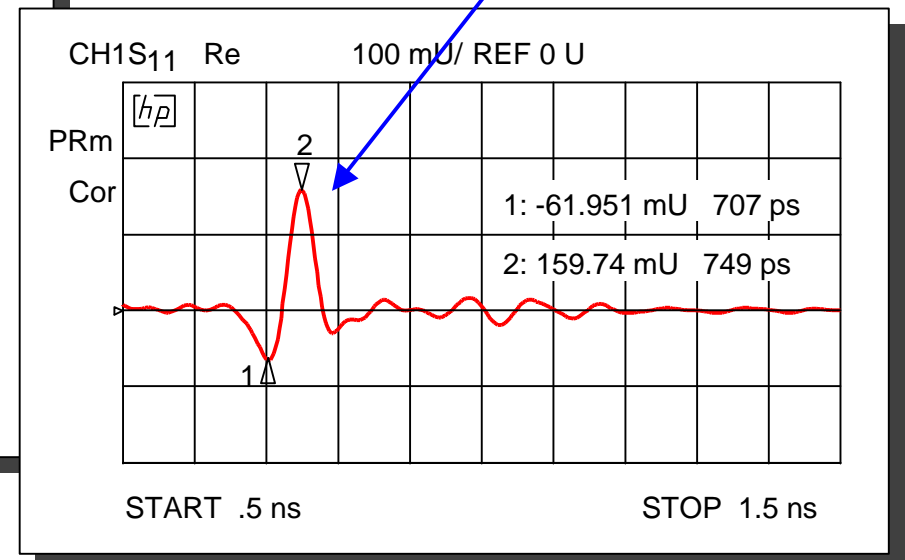
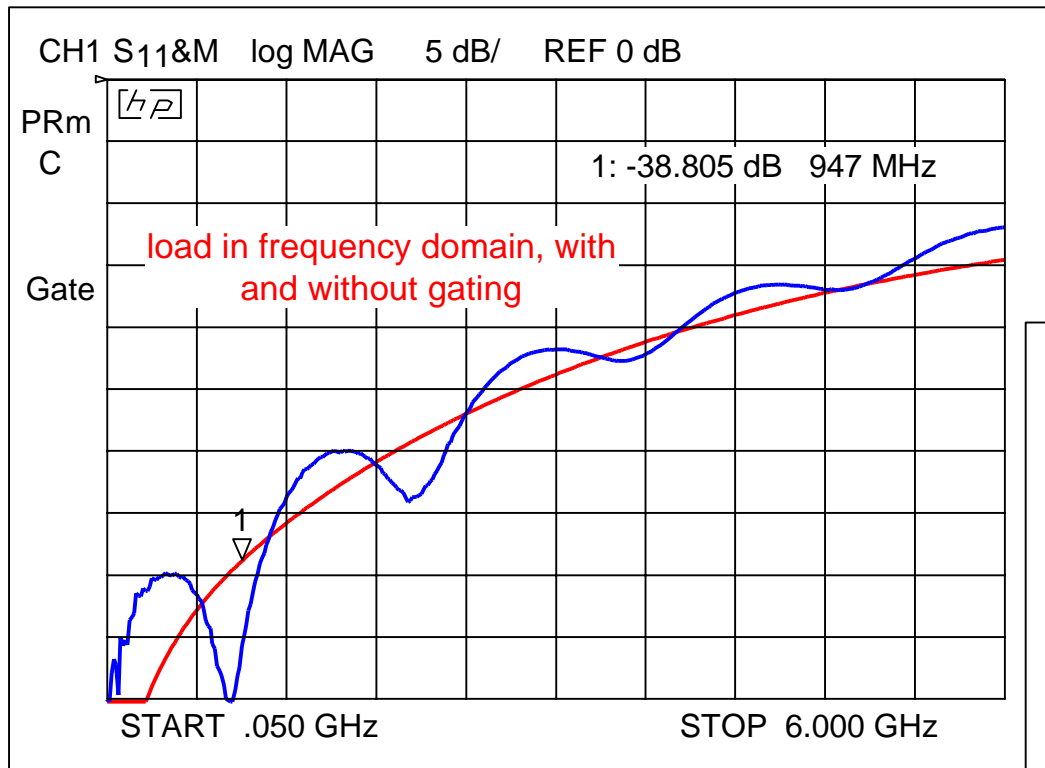


TDR Basics Using a Network Analyzer

- start with broadband frequency sweep (often requires microwave VNA)
- inverse FFT to compute time domain
- resolution inversely proportionate to frequency span



Time Domain Gating



- use time domain gating to see load reflections independent from fixture
- use time domain to compensate for imperfect load (e.g. try to cancel out inductance)

Ten Steps for Performing TDR

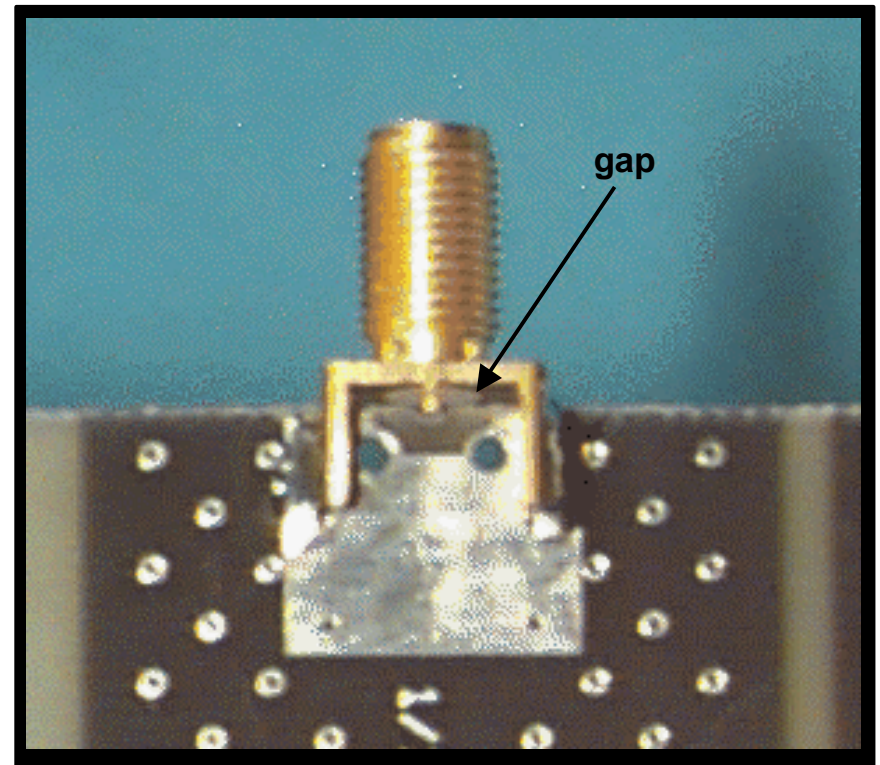
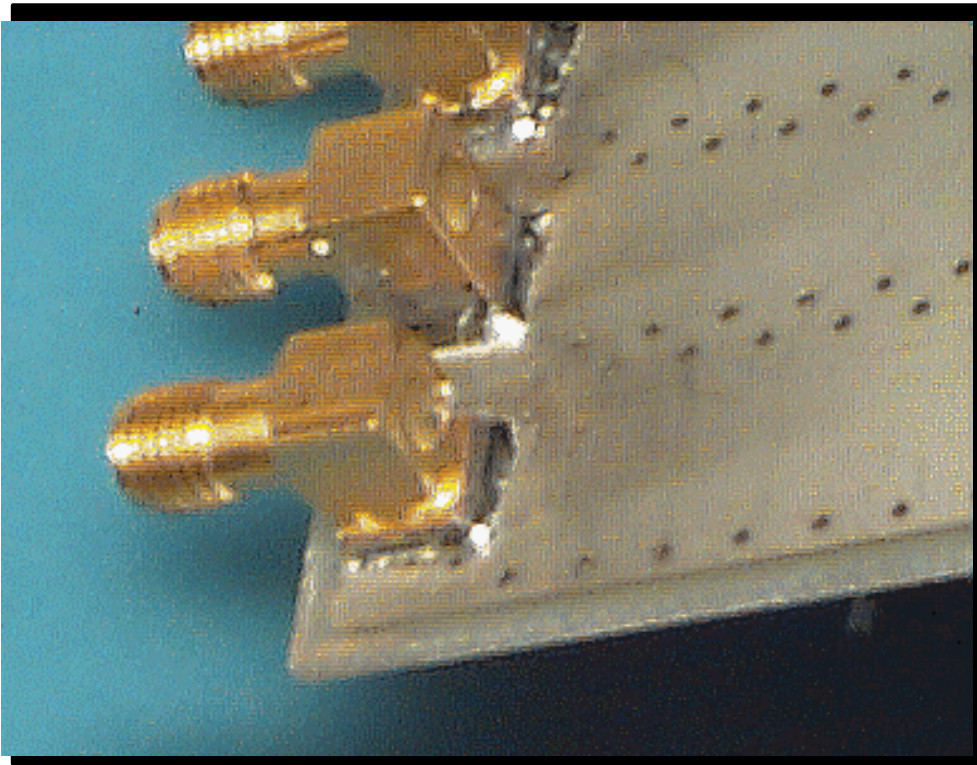
1. Set up desired frequency range
(need wide span for good spatial resolution)
2. Under SYSTEM, transform menu, press "set freq low pass"
3. Perform one- or two-port calibration
4. Select S11 measurement *
5. Turn on transform (low pass step) *
6. Set format to real *
7. Adjust transform window to trade off rise time with ringing and overshoot *
8. Adjust start and stop times if desired
9. For gating:
 - set start and stop frequencies for gate
 - turn gating on *
 - adjust gate shape to trade off resolution with ripple *
10. To display gated response in frequency domain
 - turn transform off (leave gating on) *
 - change format to log-magnitude *

** If using two channels (even if coupled), these parameters must be set independently for second channel*

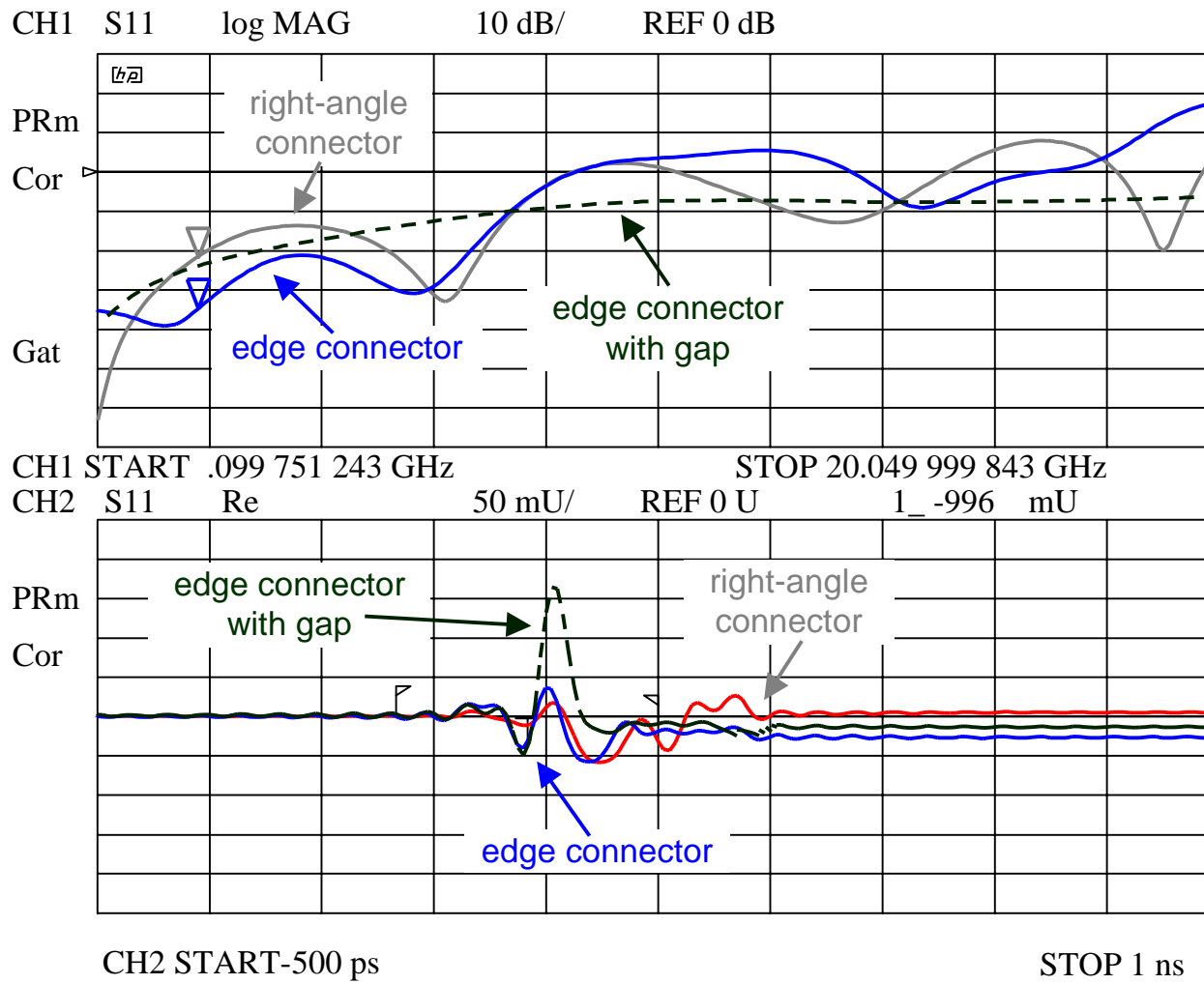


Connectors on Fixtures

- transition at the connector launch causes reflection due to mismatch
- when cal standards are inserted in fixture, connector match is removed
- when each cal standard has connectors, consistency is very important



Connector Performance



1.900 GHz

1_: -23.753 dB

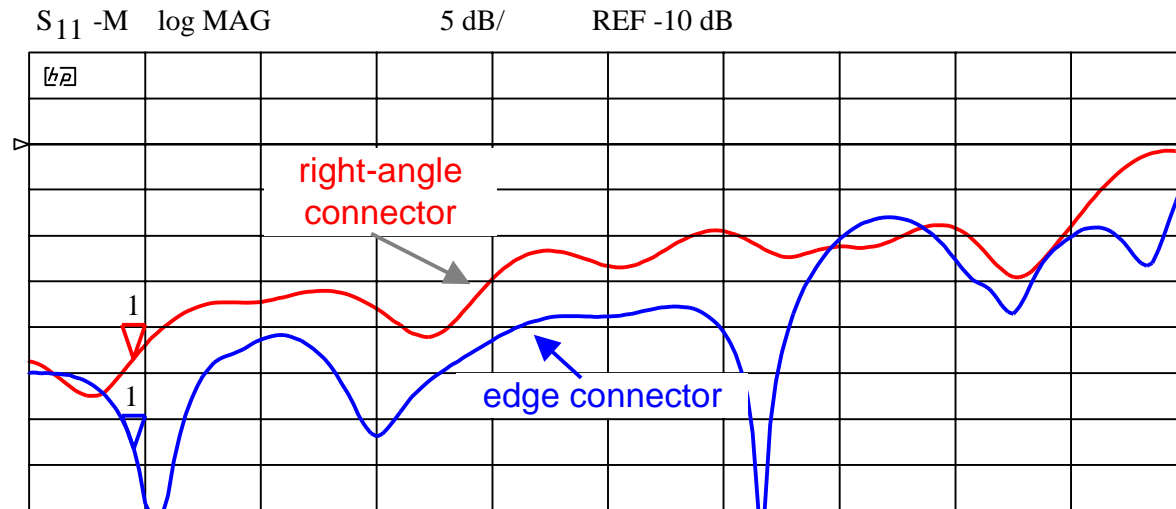
1_: -32.297 dB

frequency domain

Comparing match
of right-angle and
edge-mount connectors
(with and without gap)

time domain

Connector Consistency



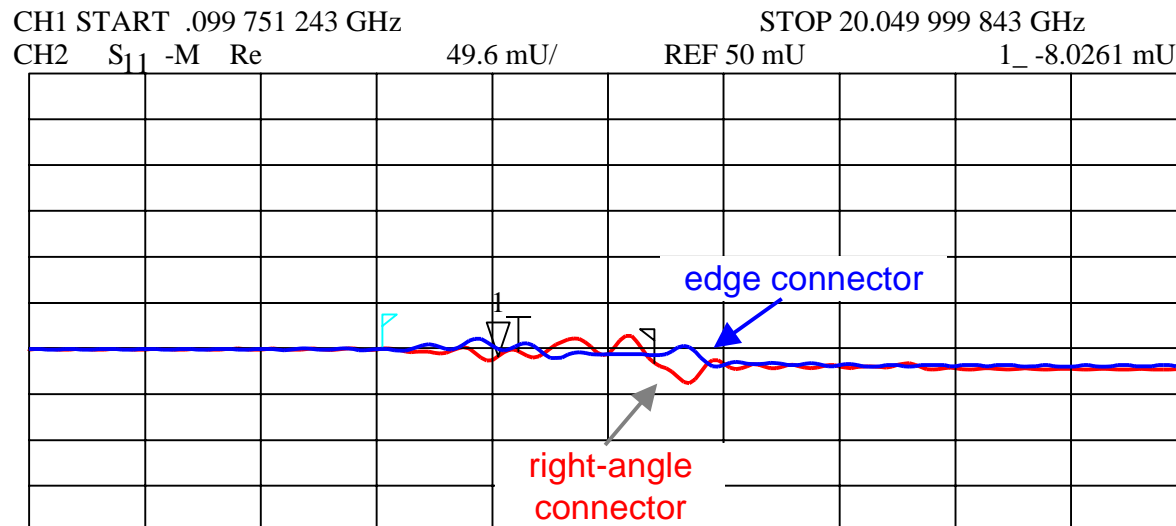
1.900 GHz

1_:-33.392 dB

1_-43.278 dB

frequency domain

Use [data - memory]
to check consistency
of connectors

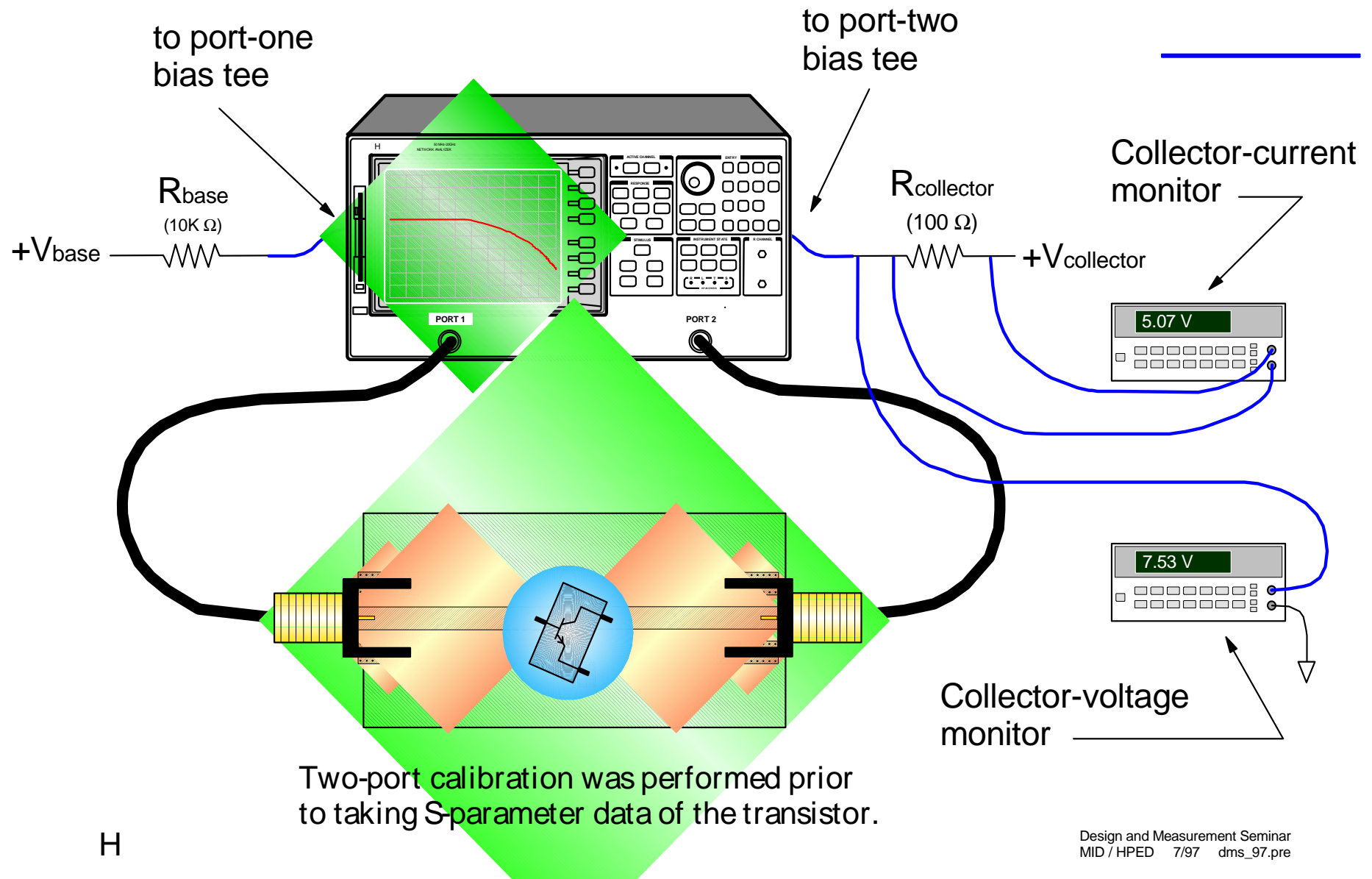


time domain

CH2 START-500 ps

STOP 1 ns

Transistor Bias Example



Linear versus Non-Linear Models

```
!Freq.[Hz] MagS11[dB] PhaseS11[DEG] MagS21[dB] PhaseS21[DEG] MagS12[dB] PhaseS12[DEG]
300000 -5.986E-07 -1.151E-02 -7.394E+01 8.997E+01 -7.394E+01 8.997E+01 -5.986E-07 -1.151E-02
315229 -6.384E-07 -1.210E-02 -7.351E+01 8.997E+01 -7.351E+01 8.997E+01 -6.384E-07 -1.210E-02
331231 -6.812E-07 -1.271E-02 -7.308E+01 8.997E+01 -7.308E+01 8.997E+01 -6.812E-07 -1.271E-02
348046 -7.273E-07 -1.336E-02 -7.265E+01 8.997E+01 -7.265E+01 8.997E+01 -7.273E-07 -1.336E-02
365714 -7.769E-07 -1.403E-02 -7.222E+01 8.997E+01 -7.222E+01 8.997E+01 -7.769E-07 -1.403E-02
384279 -8.303E-07 -1.475E-02 -7.179E+01 8.997E+01 -7.179E+01 8.997E+01 -8.303E-07 -1.475E-02
403787 -8.879E-07 -1.550E-02 -7.136E+01 8.997E+01 -7.136E+01 8.997E+01 -8.879E-07 -1.550E-02
424285 -9.501E-07 -1.628E-02 -7.093E+01 8.997E+01 -7.093E+01 8.997E+01 -9.501E-07 -1.628E-02
445823 -1.017E-06 -1.711E-02 -7.050E+01 8.997E+01 -7.050E+01 8.997E+01 -1.017E-06 -1.711E-02
468455 -1.090E-06 -1.798E-02 -7.007E+01 8.997E+01 -7.007E+01 8.997E+01 -1.090E-06 -1.798E-02
492235 -1.168E-06 -1.889E-02 -6.964E+01 8.997E+01 -6.964E+01 8.997E+01 -1.168E-06 -1.889E-02
517223 -1.252E-06 -1.985E-02 -6.921E+01 8.997E+01 -6.921E+01 8.997E+01 -1.252E-06 -1.985E-02
543479 -1.344E-06 -2.086E-02 -6.878E+01 8.997E+01 -6.878E+01 8.997E+01 -1.344E-06 -2.086E-02
```

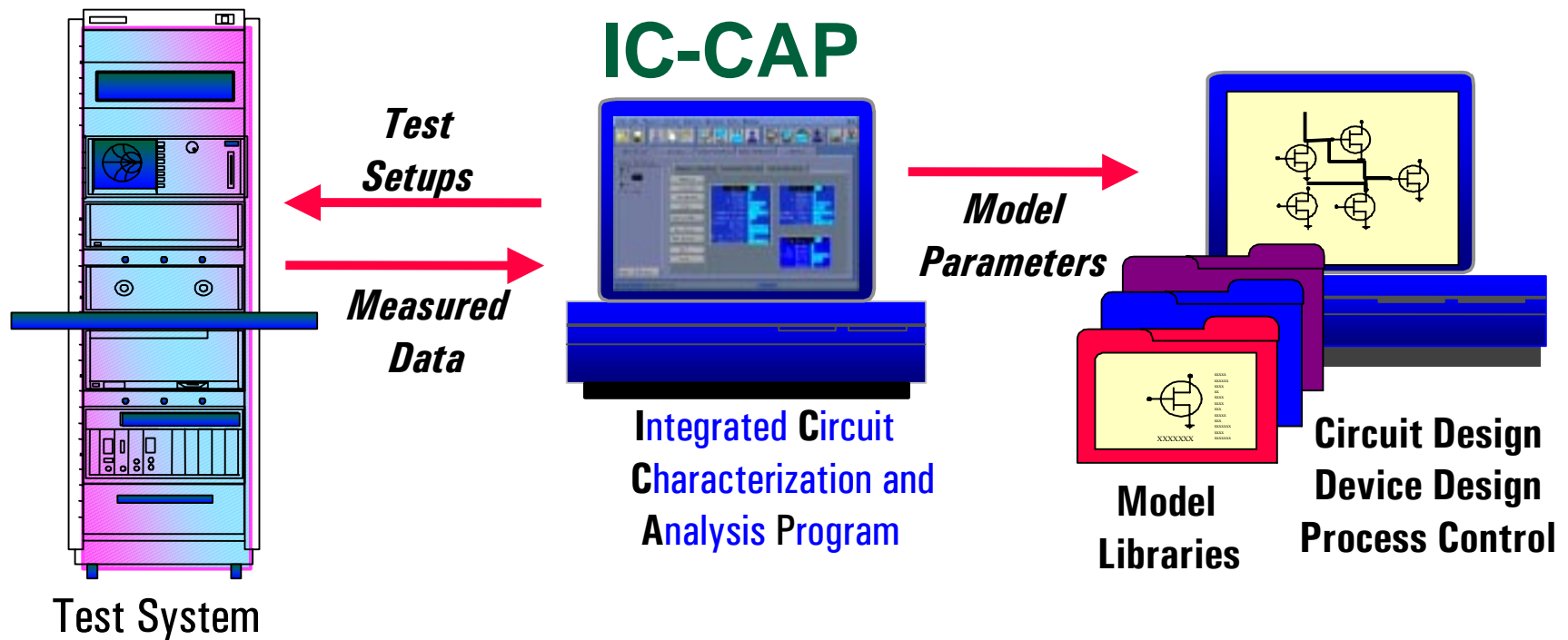
- valid for one bias condition
- valid for small signal



- device completely characterized
- valid for all bias conditions
- valid for non-linear operation

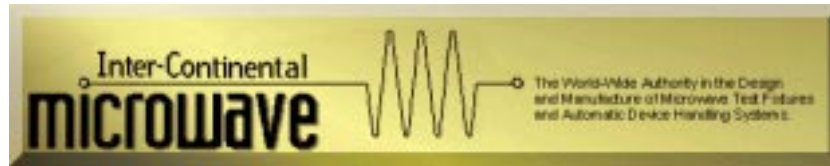
$$I_{be} = (I_{Bbif}(\exp(V_{be}/N_{bf}V_T) - 1.0)) + I_{se}(\exp(V_{be}/(N_{ex}V_T)) - 1.0)$$

IC-CAP: Integrated Circuit Characterization and Analysis Program



References and More Information

- ***Fixtures - www.icmicrowave.com***



- ***TDR - www.hp.com***



- ***IC-CAP - www.hp.com***

