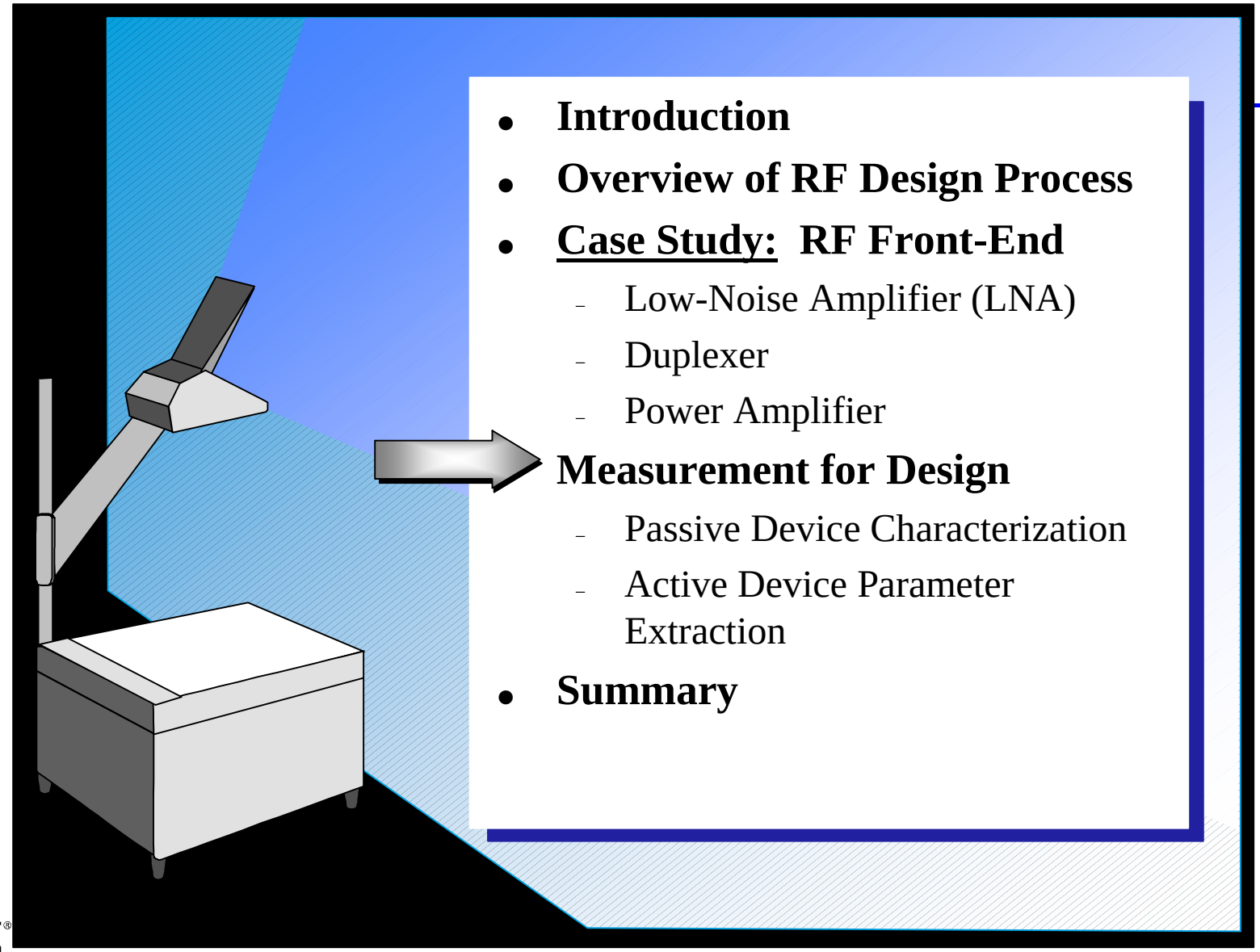
Agenda



- **Introduction**
- **Overview of RF Design Process**
- **Case Study: RF Front-End**
  - Low-Noise Amplifier (LNA)
  - Duplexer
  - Power Amplifier
- **Measurement for Design**
  - Passive Device Characterization
  - Active Device Parameter Extraction
- **Summary**

Power Amp Design

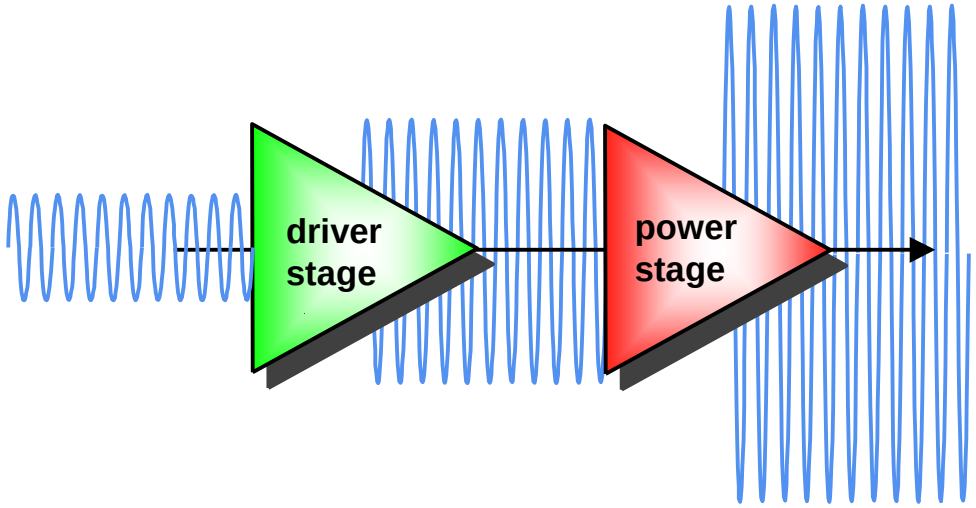
1.88 GHz PCS-Band Amplifier

- Gain > +24 dB
- 1-dB-compression > +25 dBm
- Psat > +27 dBm

Main challenge: designing for maximum power output

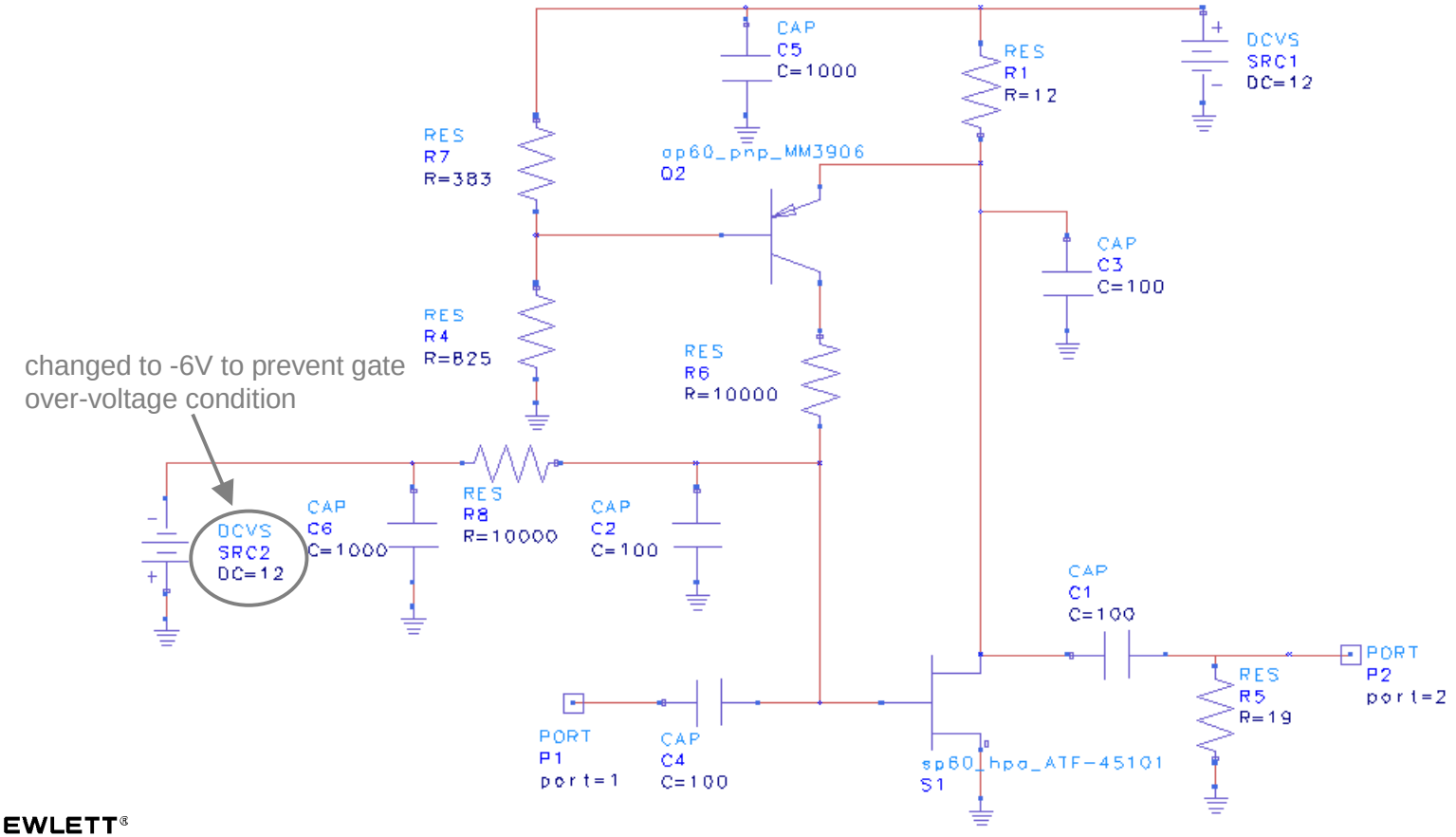
During brainstorm process, decided:

- two stages needed to get desired gain
- stage one:
  - silicon transistor
  - passive bias
- stage two:
  - power FET
  - active bias



Bias Considerations - Active vs. Passive

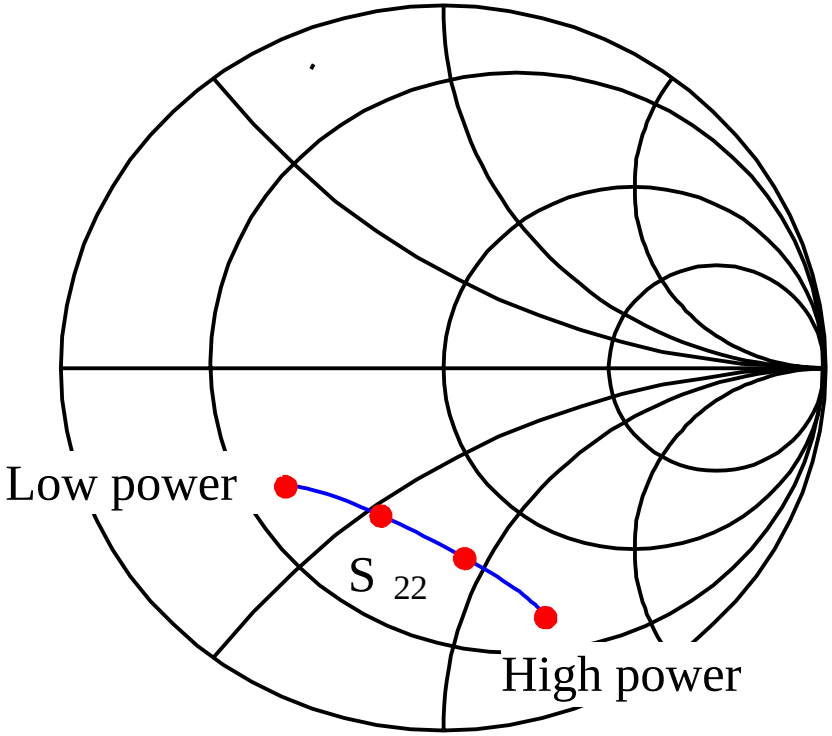
- passive - simpler, less space, cheaper but not as well controlled
- active - extra circuitry, but more repeatable
- hint: watch out for over-biasing junctions (FET gate-bias example)



HEWLETT® PACKARD

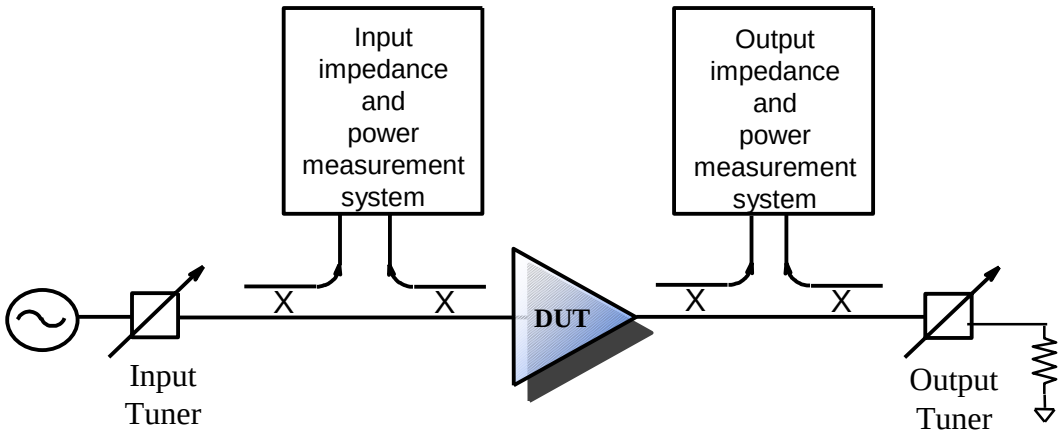
Designing the Output Stage for Maximum Output Power

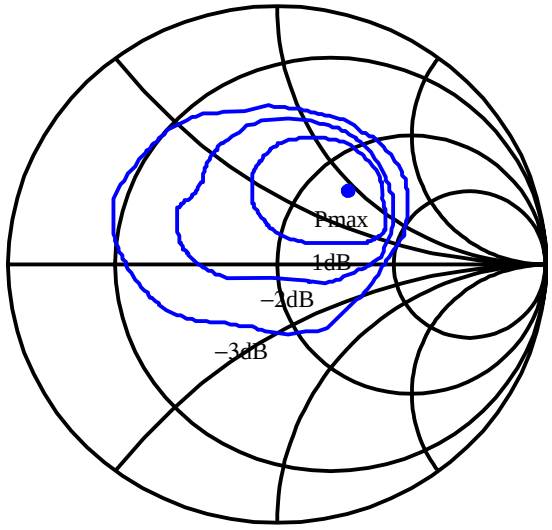
- output impedance varies as function of output power
- ideal impedance exists for maximum output power
- two technique provides information for output-stage matching
  - load-pull technique
  - load-line analysis



Load-Pull Technique

- vary magnitude and phase of load presented to circuit
- power output is measured at each impedance point
- can use behavioral model (based on measurements)



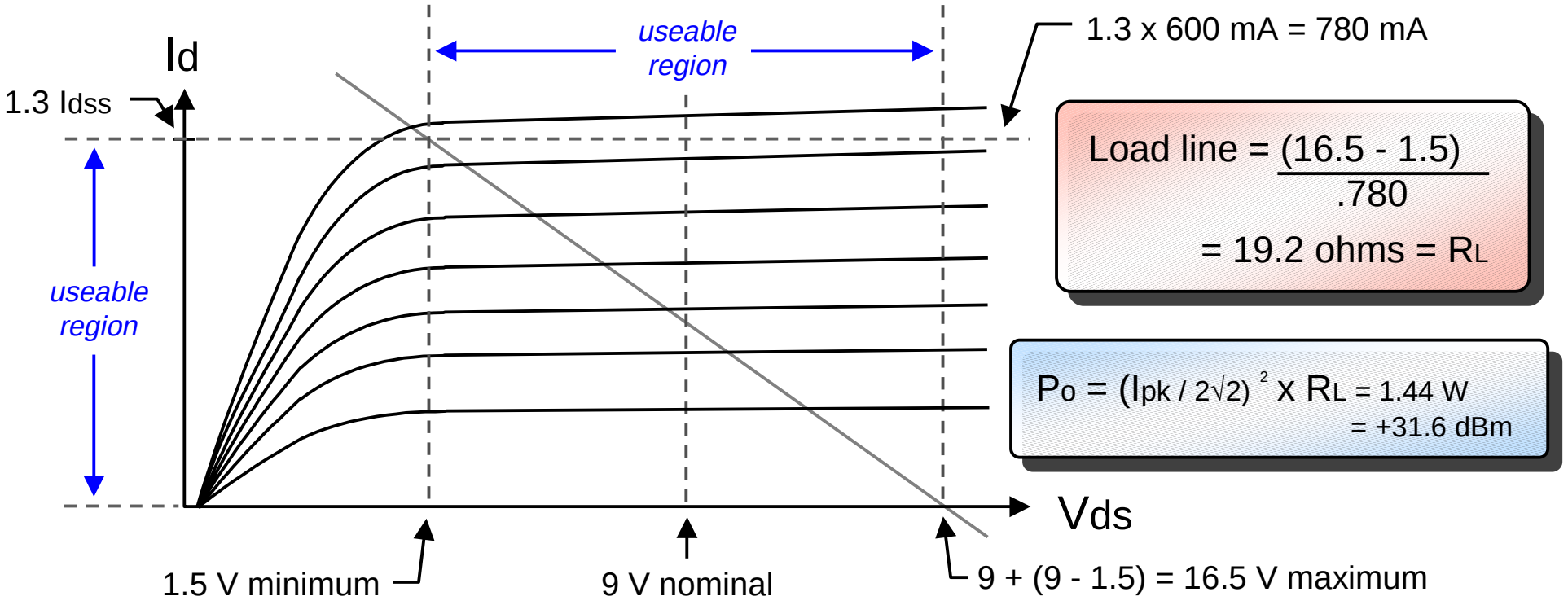


Constant output power contours versus output load impedance (input power constant)

Can be very expensive and time-intensive

Load-Line Analysis

- determines resistance that gives highest power
- current source of FET needs to be presented with this load
- should give same output match as load-pull technique



HEWLETT PACKARD

Matching to FET Output

- need to have accurate physical model of device
- parasitics must be included in matching circuit
  - include FET and package parasitics
  - assume simple parallel-output capacitance for
  - can determine C_p from chip model
- use mirror-matching technique

Output match of FET chip

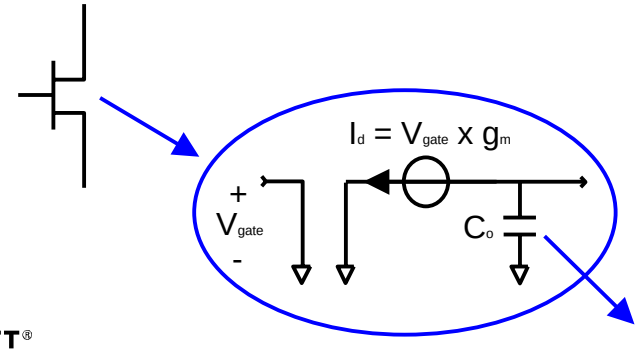
external output matching circuit

Package model

Ouput capacitance of FET

Load resistor determined from load-line analysis

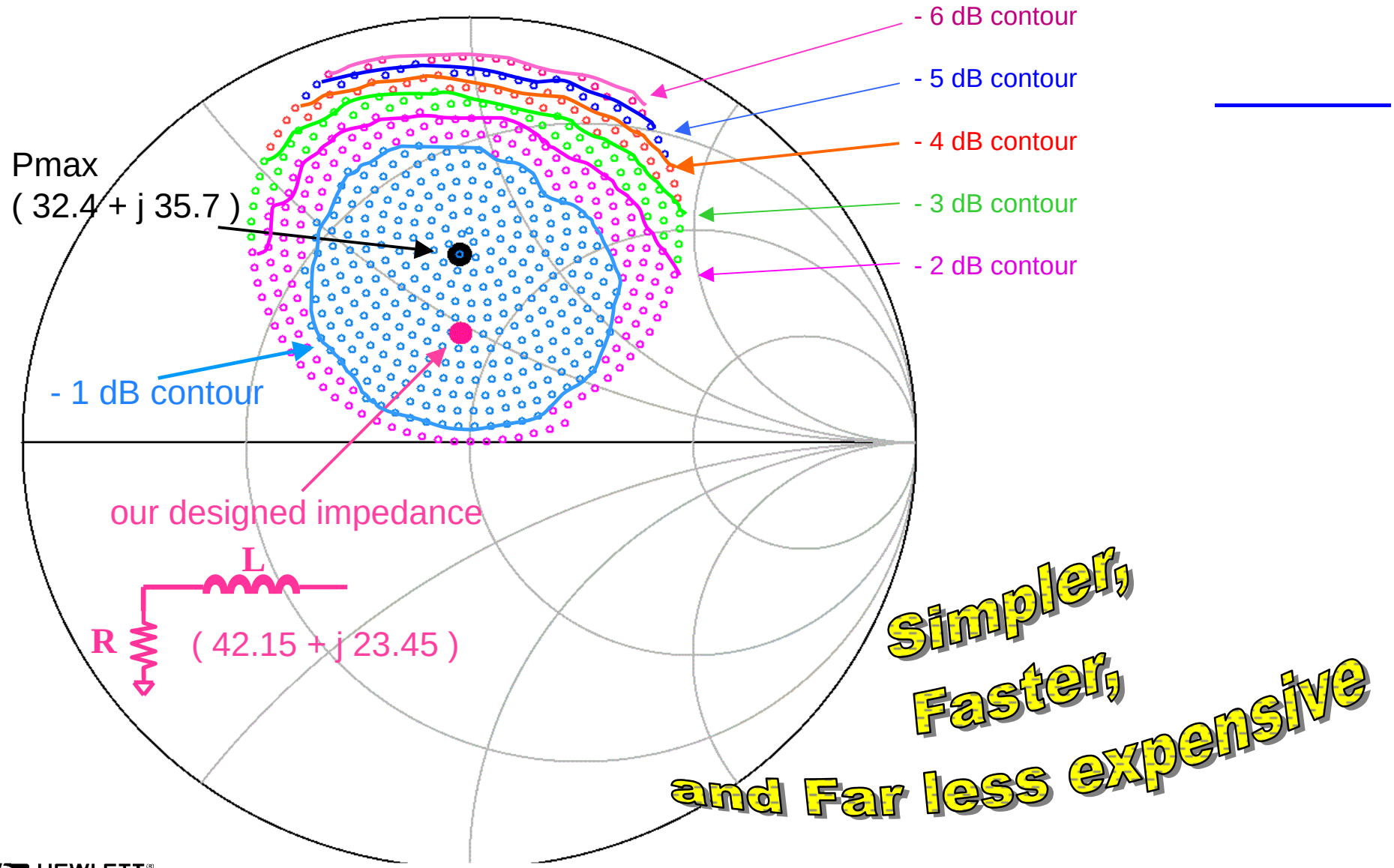
match to 50 ohms here



$Co = y / (2\pi f * 50) = 1.02$ pf

HEWLETT® PACKARD

Load-Pull Simulation

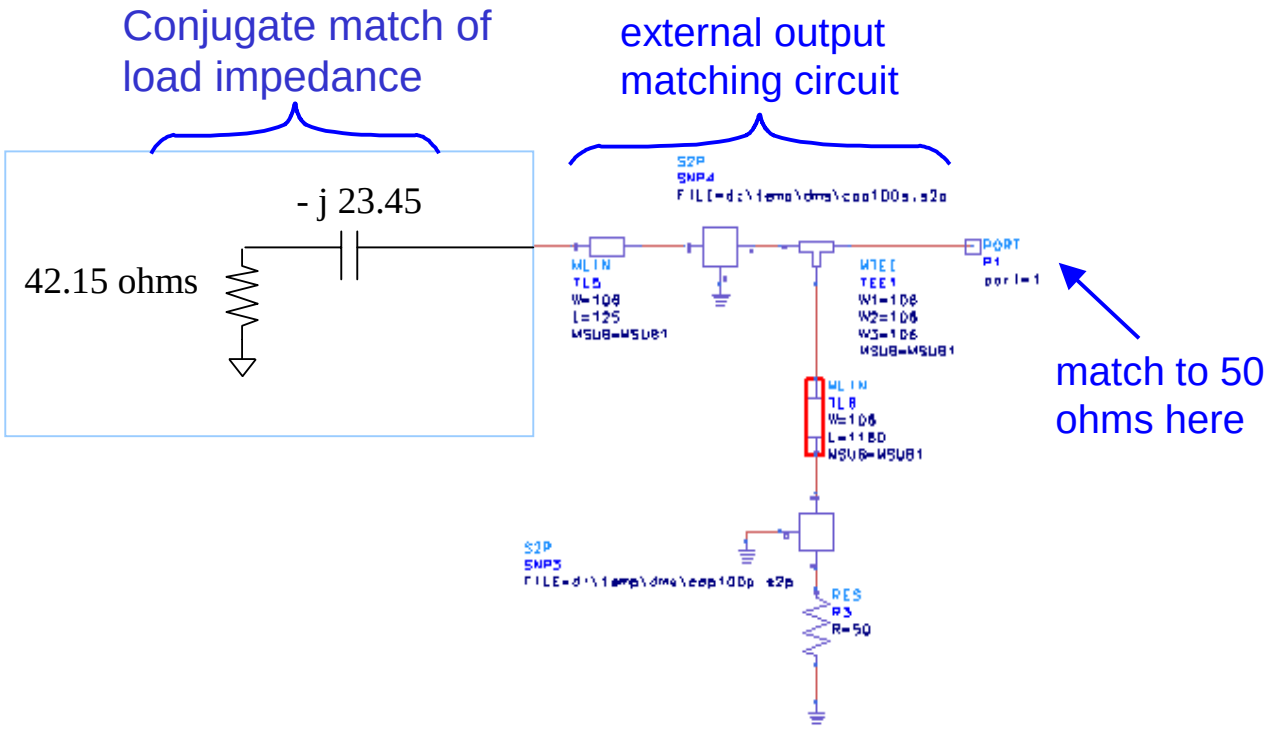


Simpler, Faster, and Far less expensive

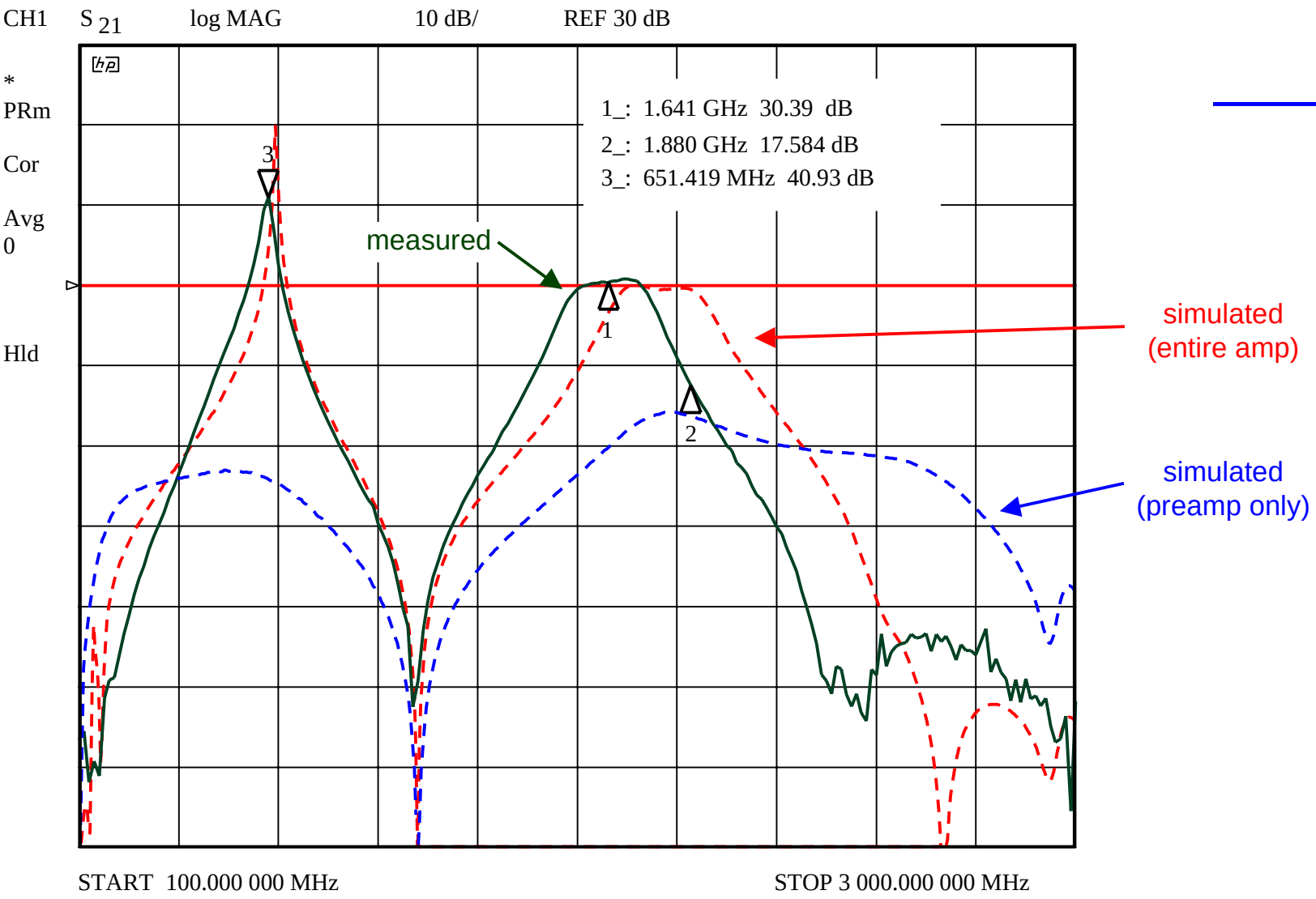
HEWLETT PACKARD

Using data from the load-pull simulation to design a matching network

- No need to model parasitics of FET or package
- Use mirror-matching technique
- Easier and faster



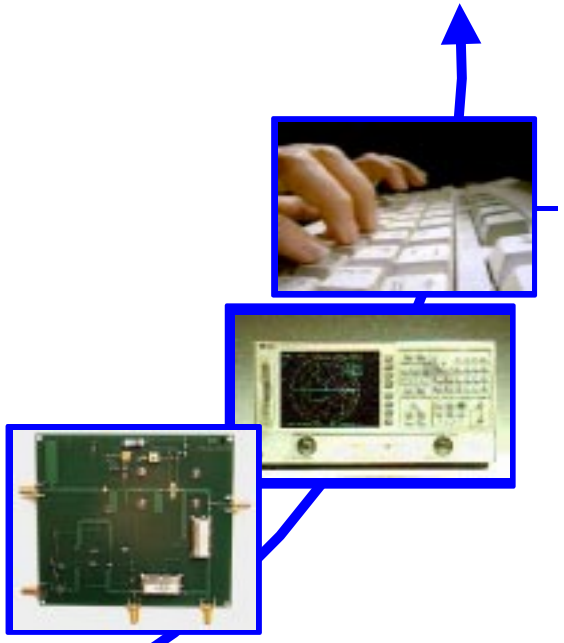
Measured Performance of First Prototype



HEWLETT PACKARD

Modifying Tips

First, verify there are no errors in the fabrication or measurement of the prototype.



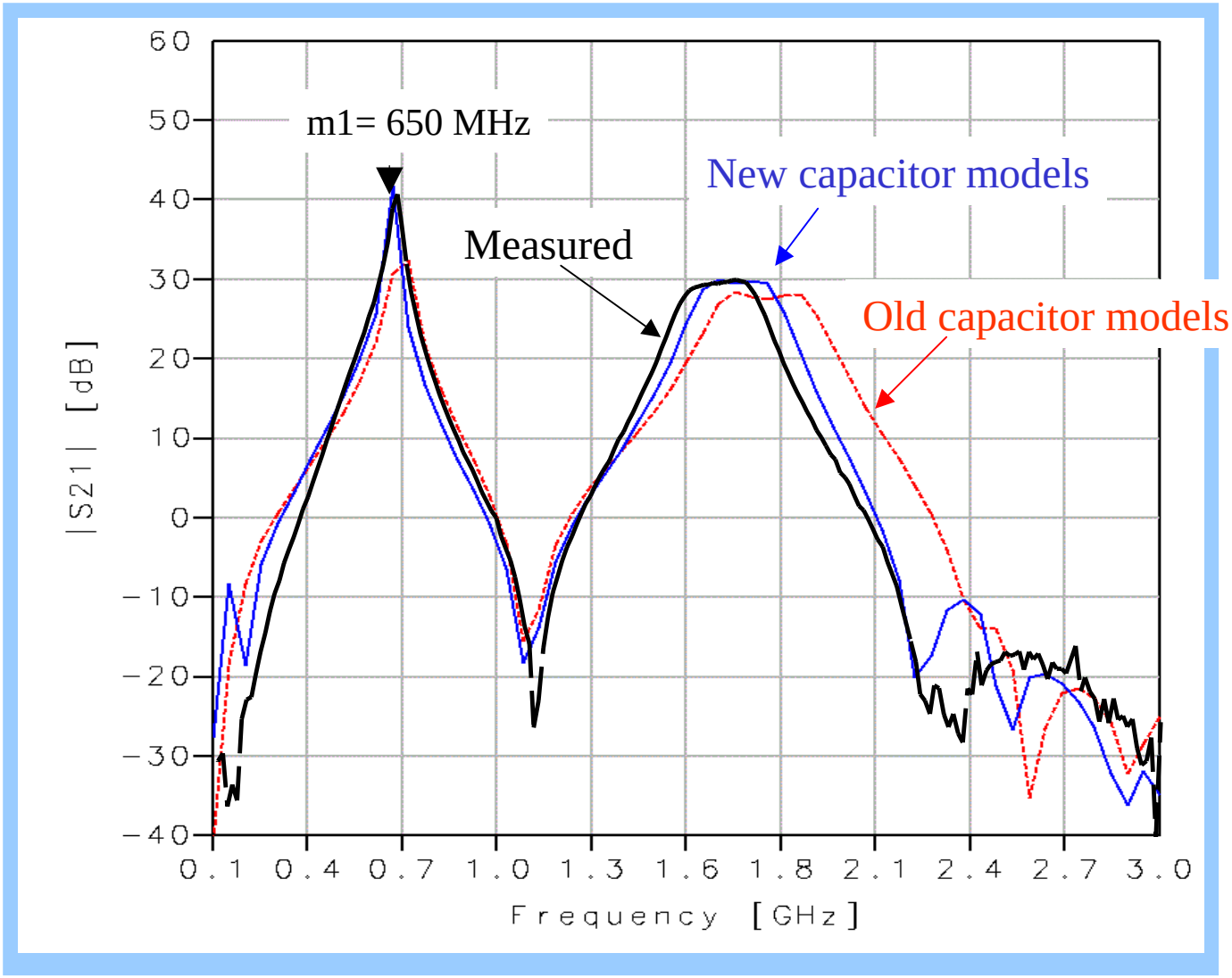
Why modify the circuit design file to match the prototype?

- Because a prototype is a very useful tool for improving the accuracy of the circuit design file
- gives good assurance that design changes will indeed improve design

Can start by,

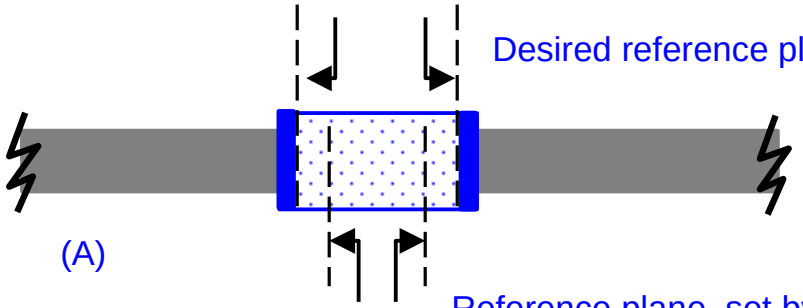
- accounting for fringing effects or discontinuities
- removing transistor and measuring only bias components
- connecting ground vias directly to the main transmission line

Modify the circuit design file



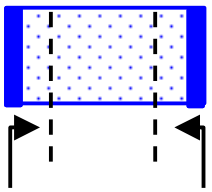
HEWLETT® PACKARD

Importance of accurate measurements



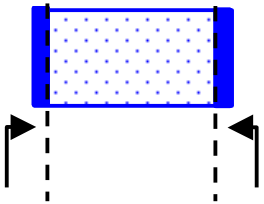
(A)

Reference plane, set by test fixture calibration



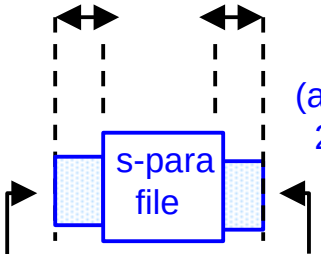
(B)

Reference plane of capacitor's measured s-parameter



(C)

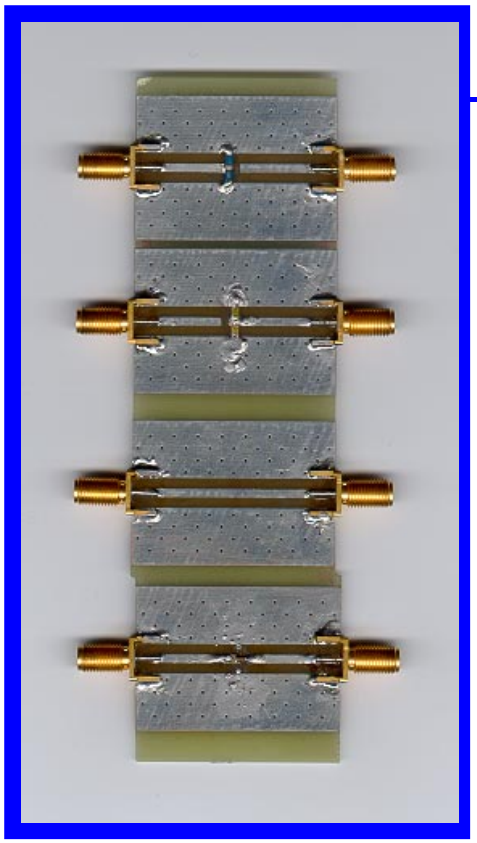
Desired reference plane of capacitor's measured s-parameter



(additional transmission line lengths, 20 mils on either side)

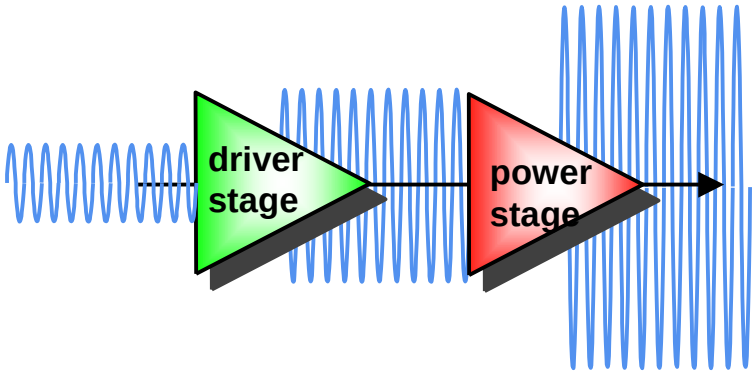
(D)

Modified s-parameter model of capacitor



test fixture

Design Refinement



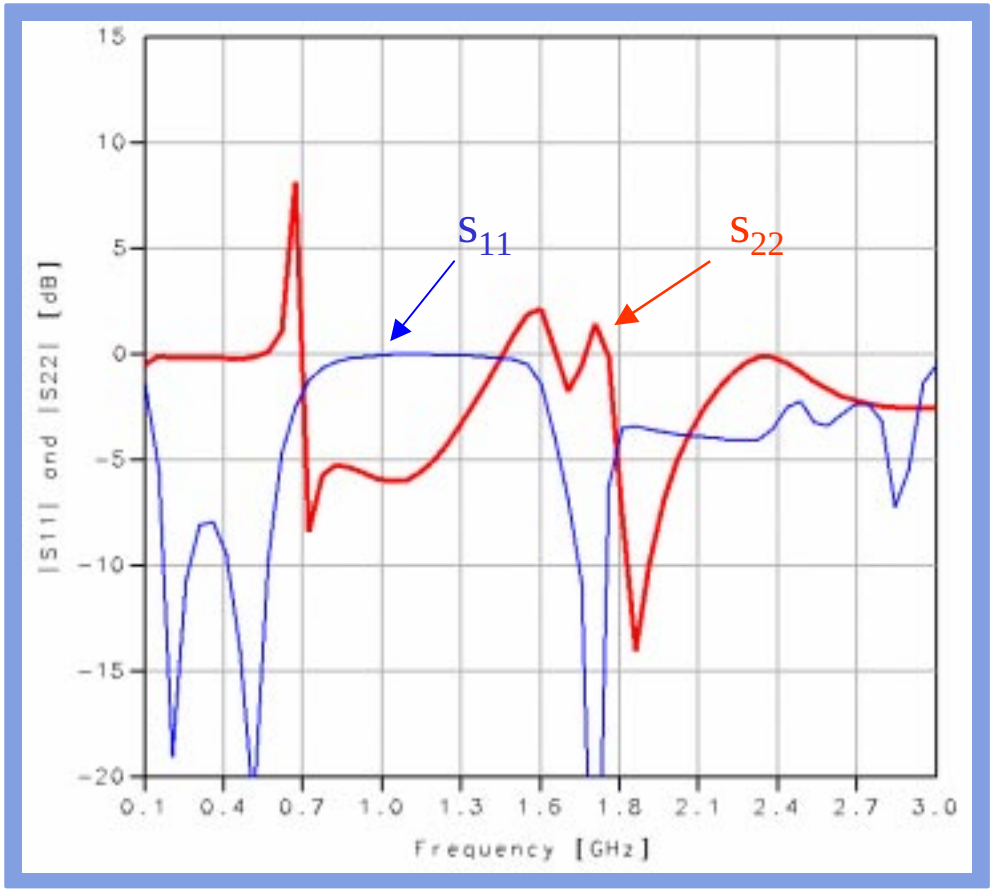
2 gain stages, oscillation can be caused by:

.. driver stage

.. power stage

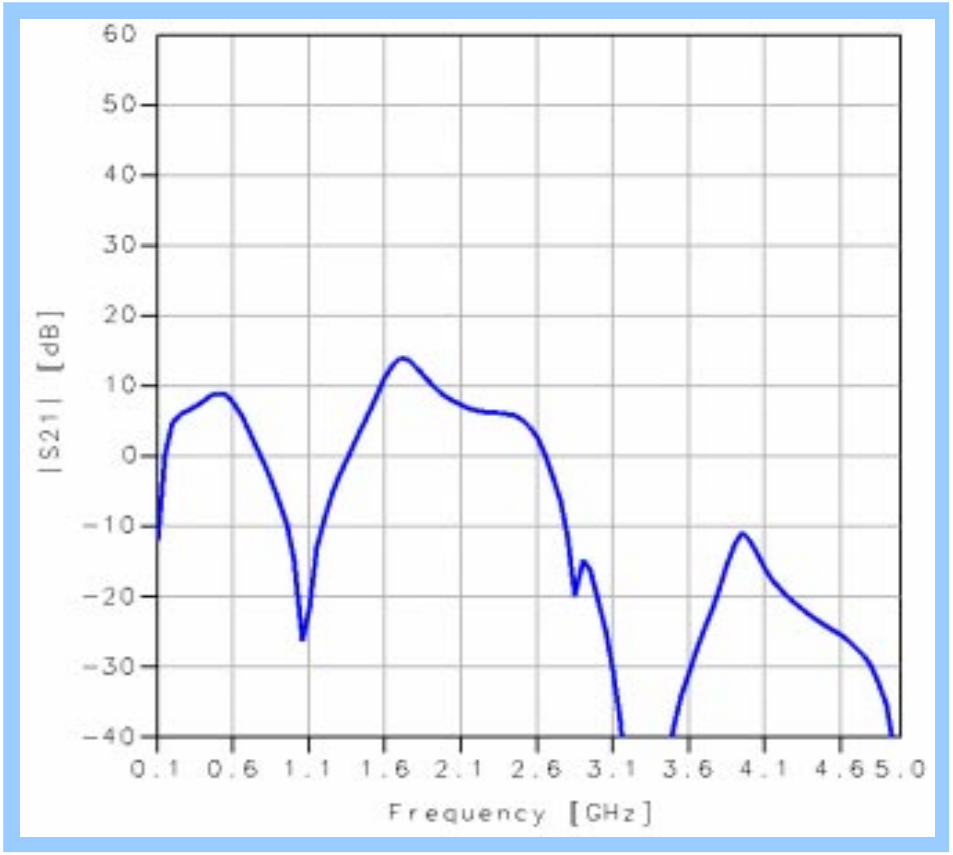
.. both stages

----> Need to separate each stage and examine

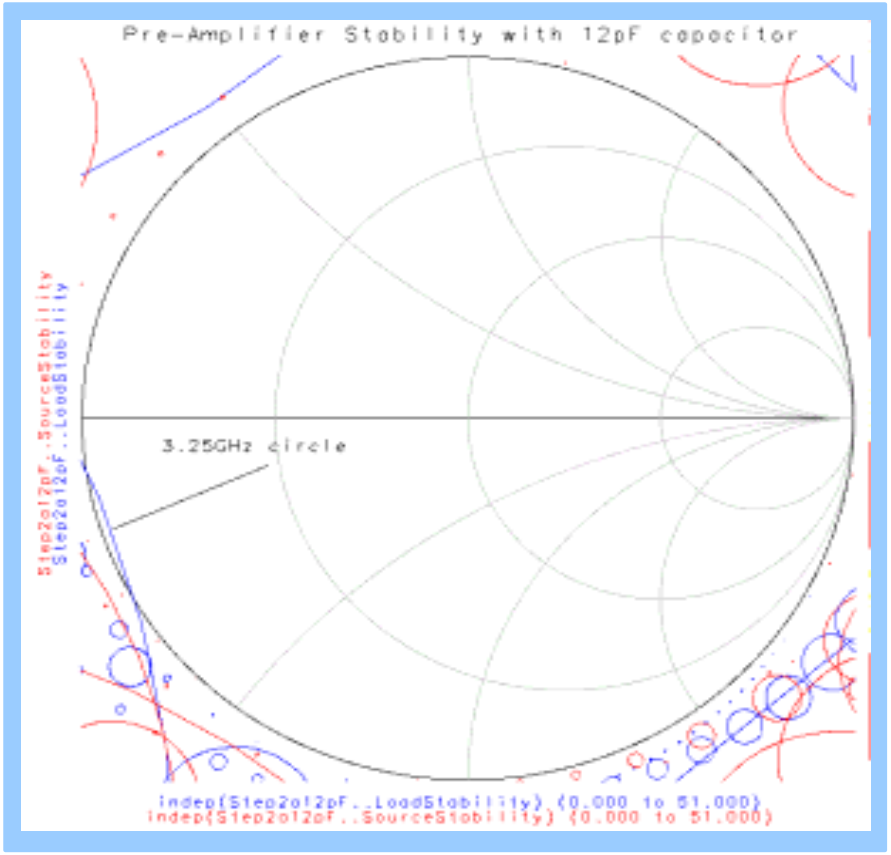


Driver Stage

Gain



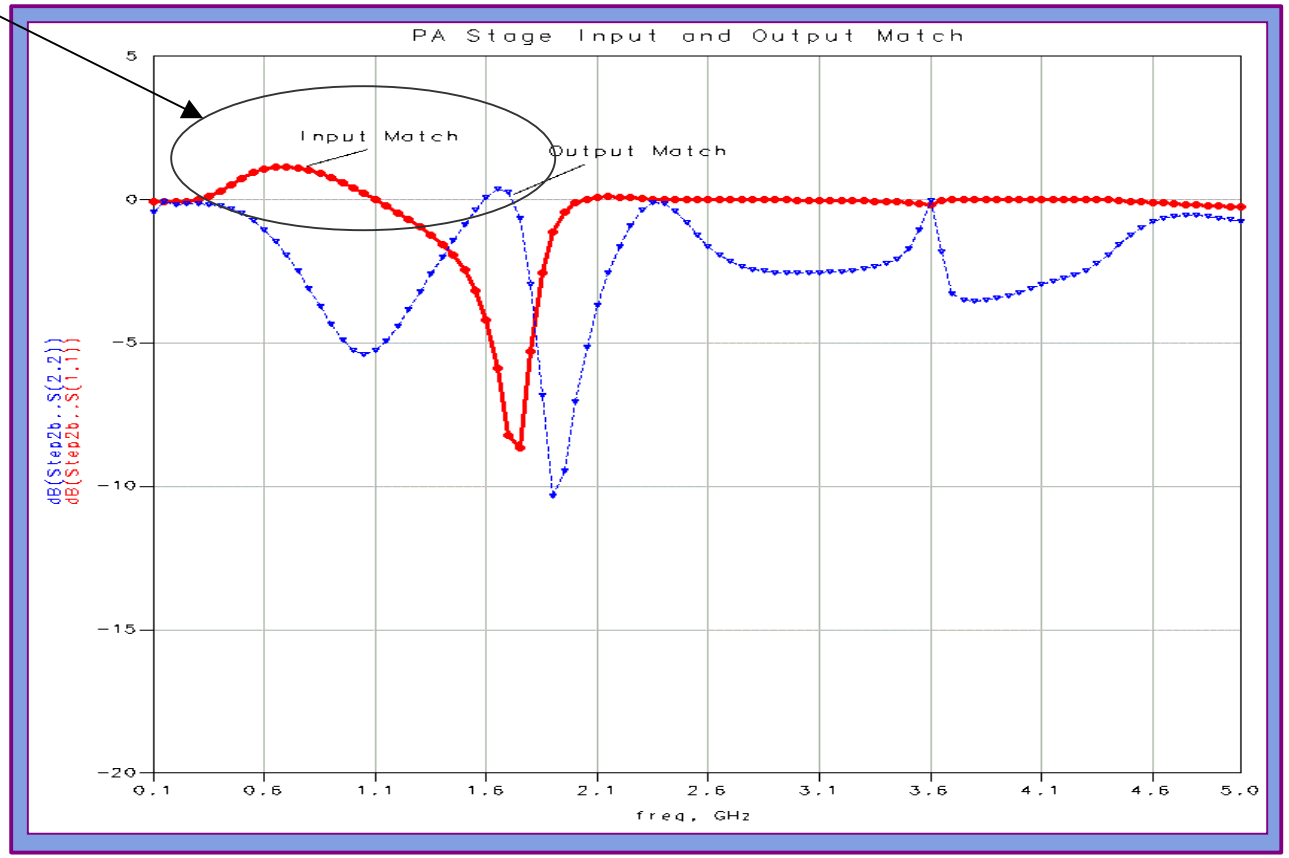
Stability Circles



HEWLETT® PACKARD

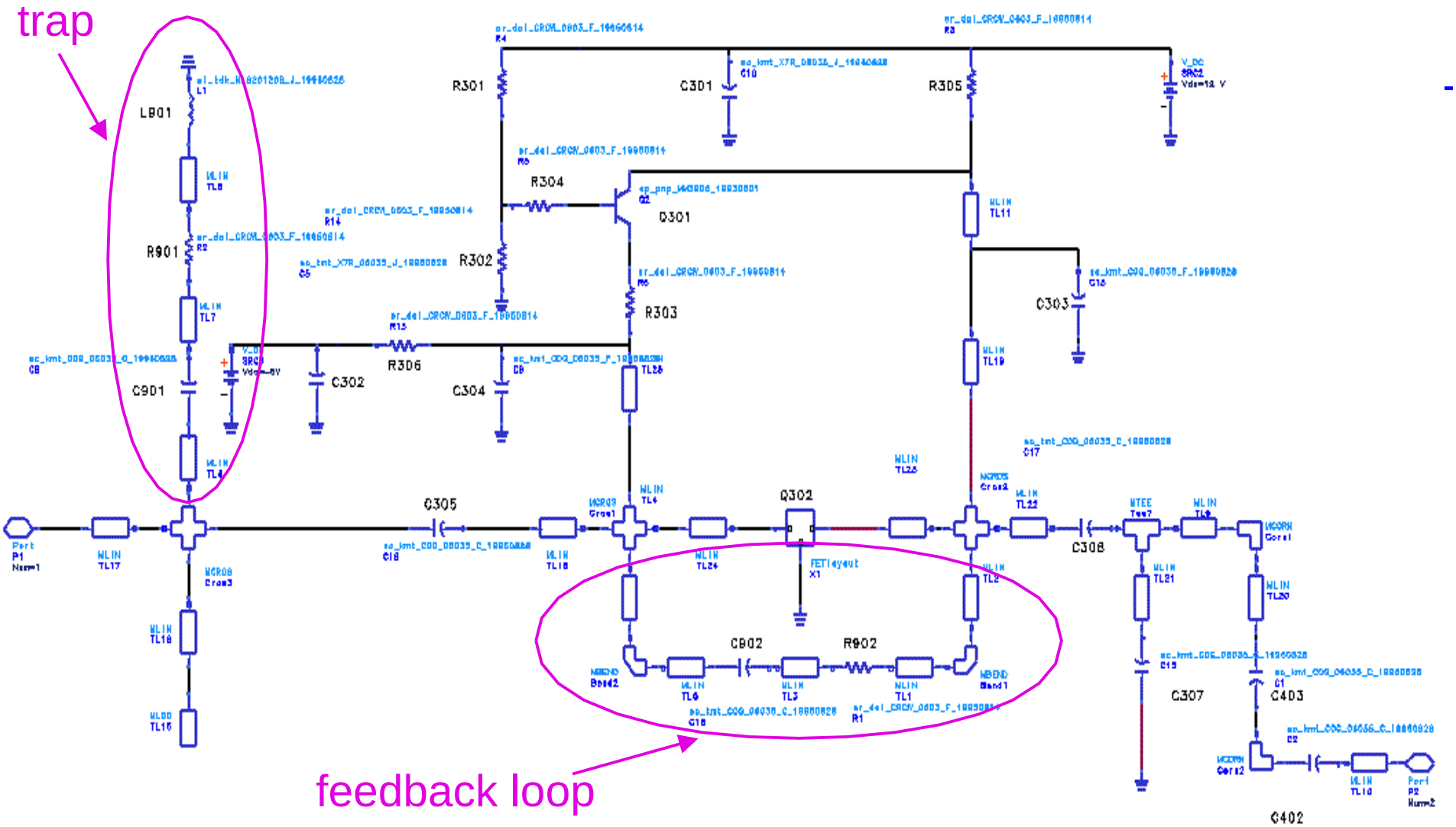
Power Stage: Input & Output Match

Potentially
Unstable



HEWLETT® PACKARD

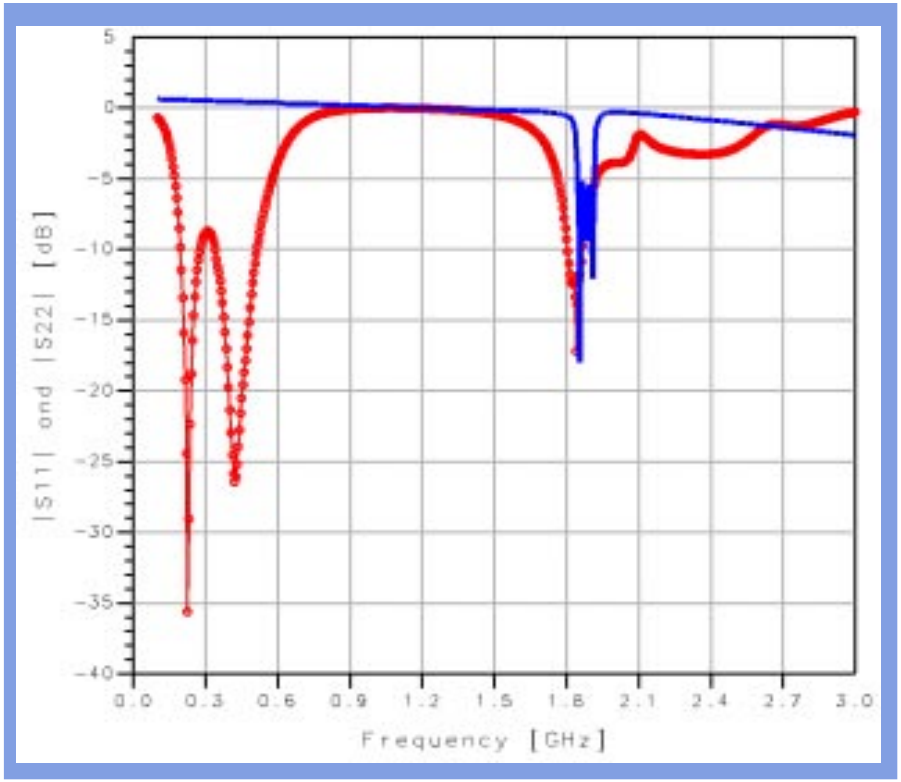
Schematic of New Power Stage



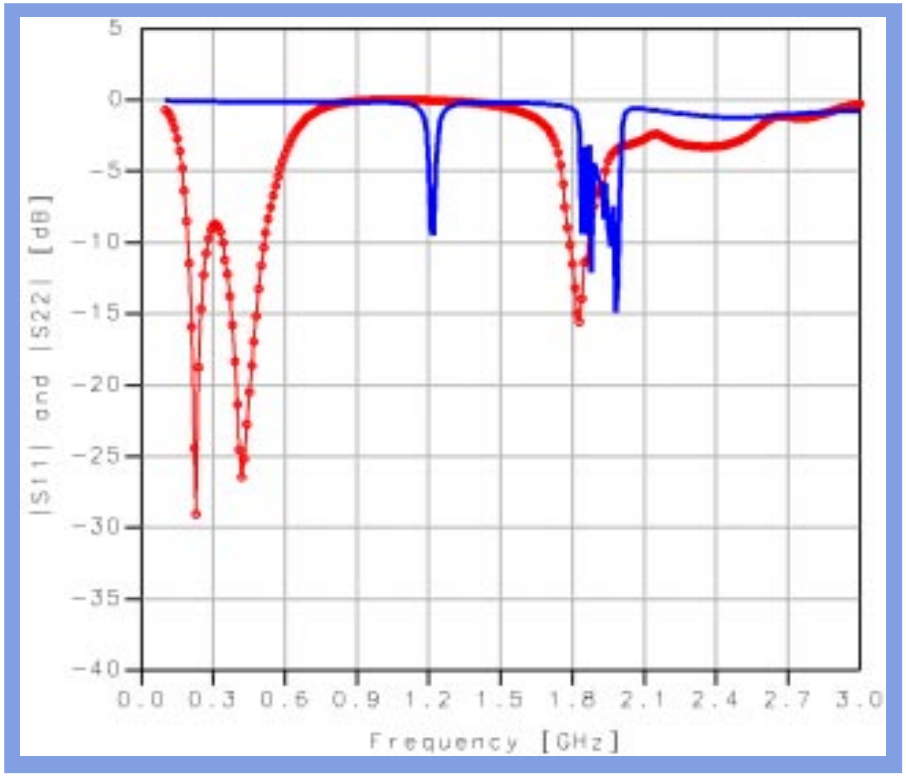
HEWLETT® PACKARD

Completed amplifier's s_{11} and s_{22} responses with duplexer filter connected

Analysis using filter s-parameter file, obtained over a narrow frequency band

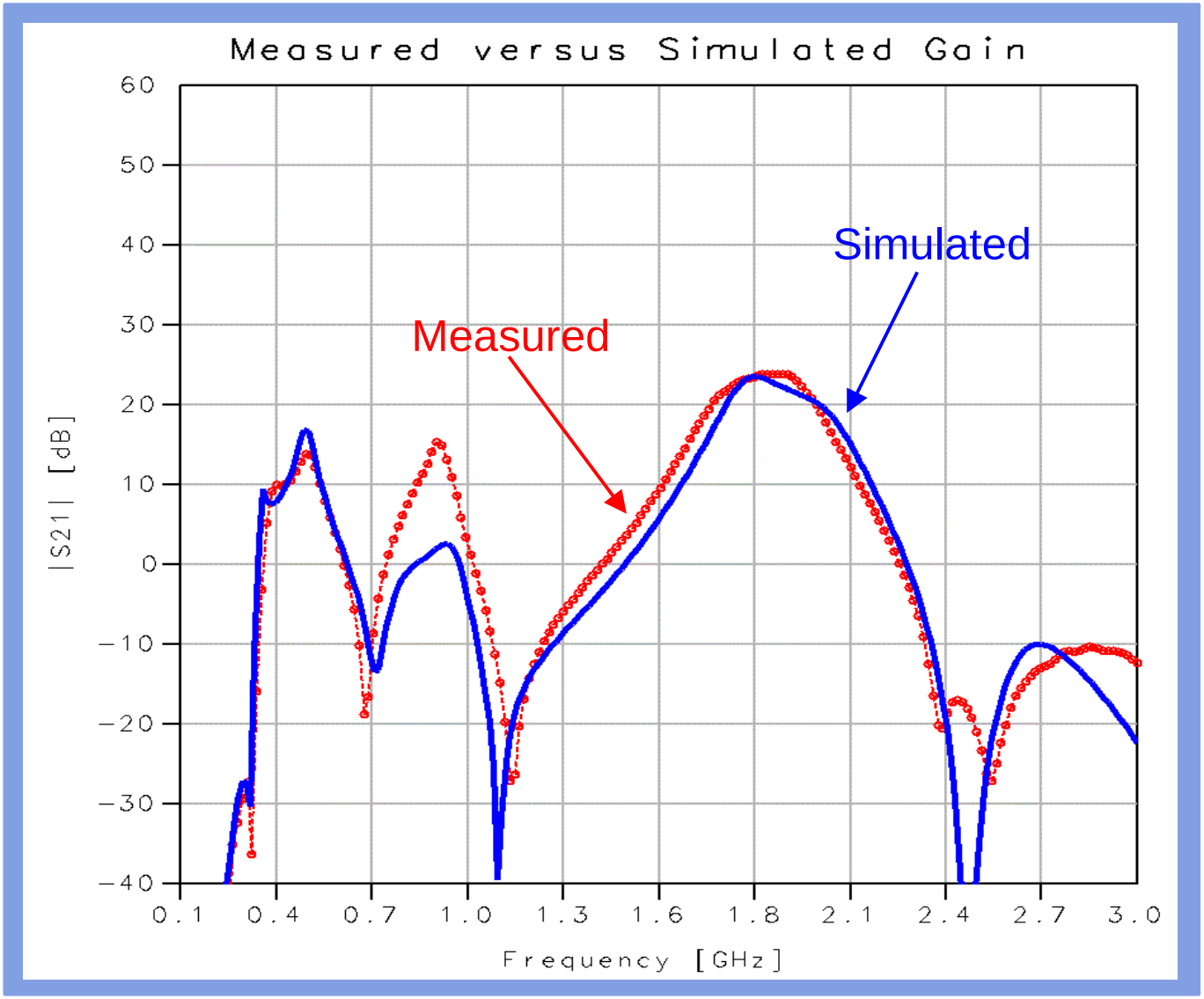


Analysis using filter s-parameter file, obtained over an appropriately wide frequency band



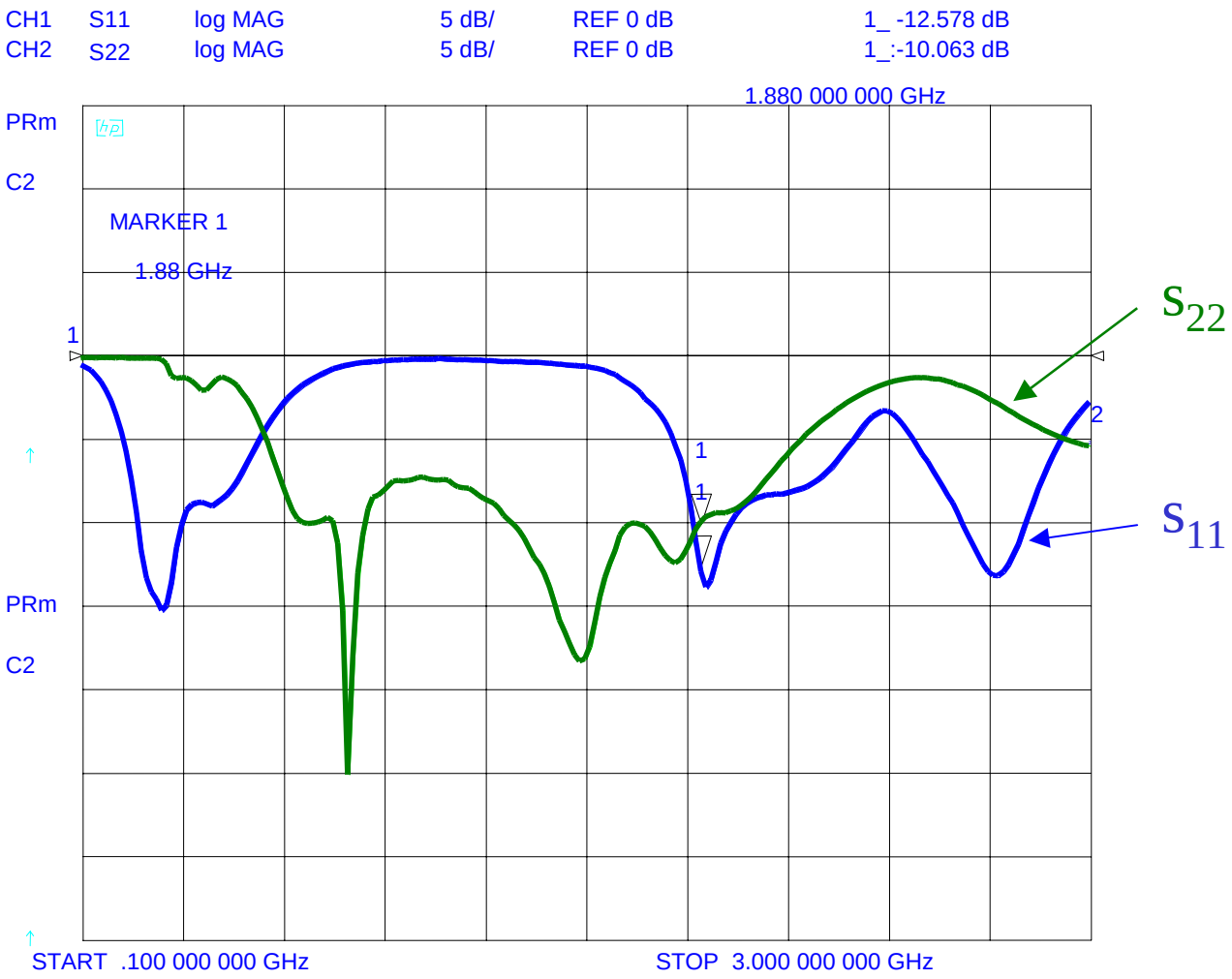
HEWLETT® PACKARD

Working Power Amplifier !



HEWLETT® PACKARD

Input and Output Match

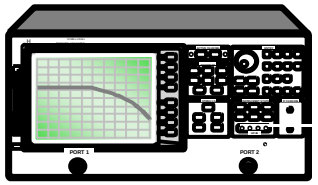


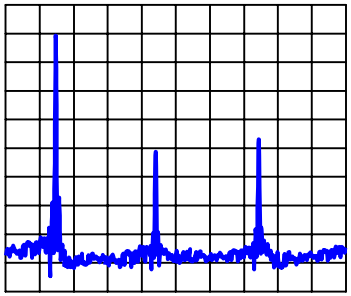
HEWLETT® PACKARD

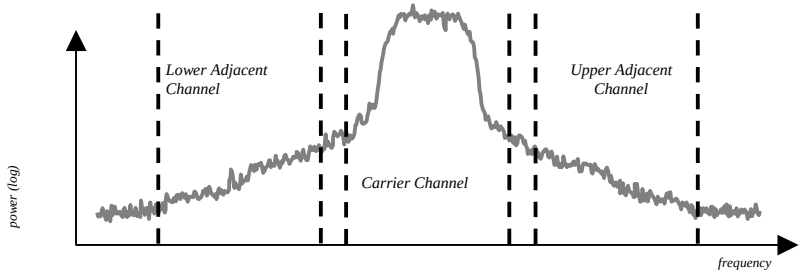
Characterizing Nonlinear Behavior

Power amplifiers require additional measurements to characterize nonlinear behavior

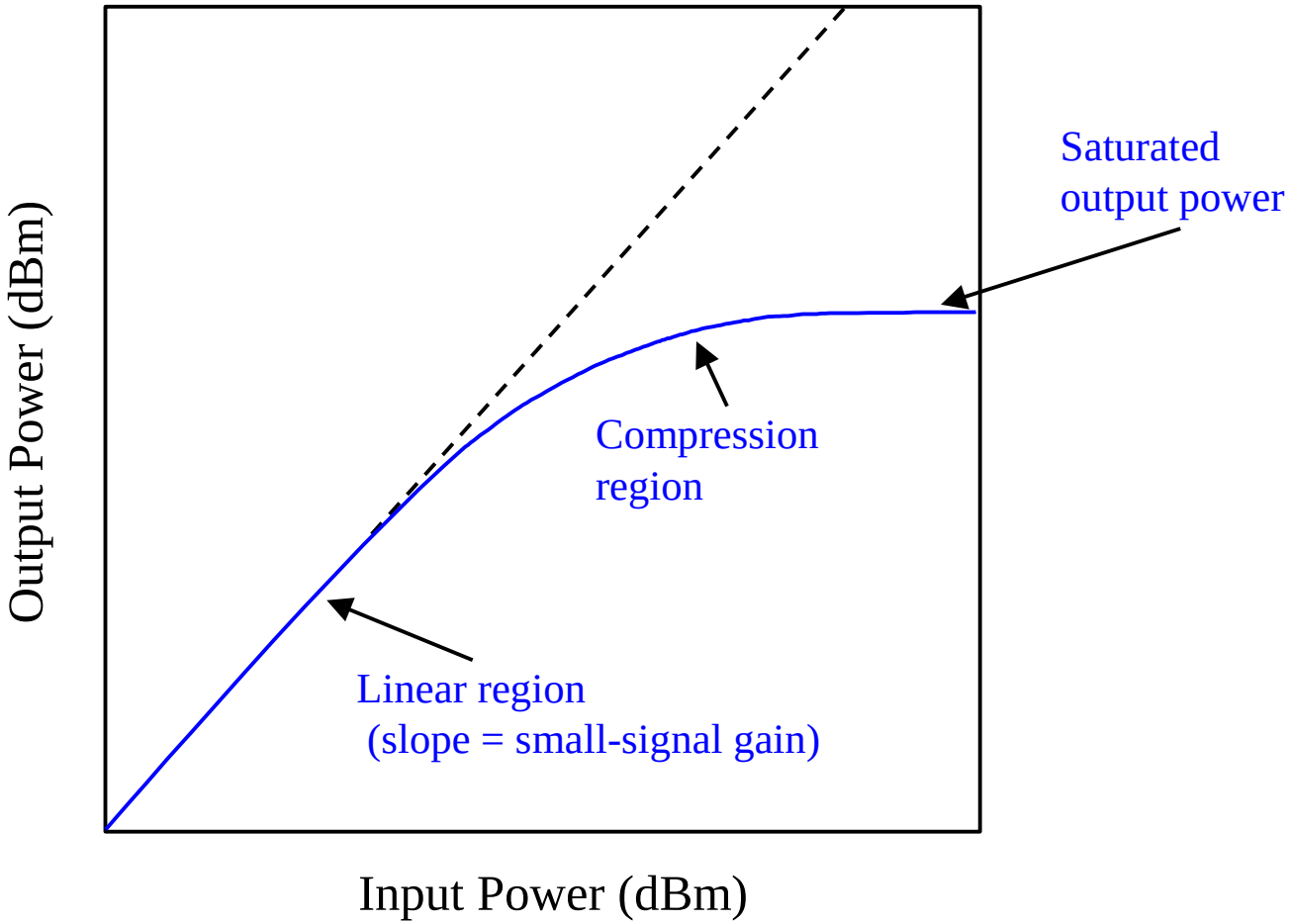
- power sweeps (using network analyzer)
  - gain compression
  - AM to PM conversion
- single-tone harmonic
  - second harmonic
  - third harmonic
- multi-tone intermodulation
  - third-order intercept using two tones
  - high-order intermodulation using many carriers
- digital modulation
  - adjacent-channel power



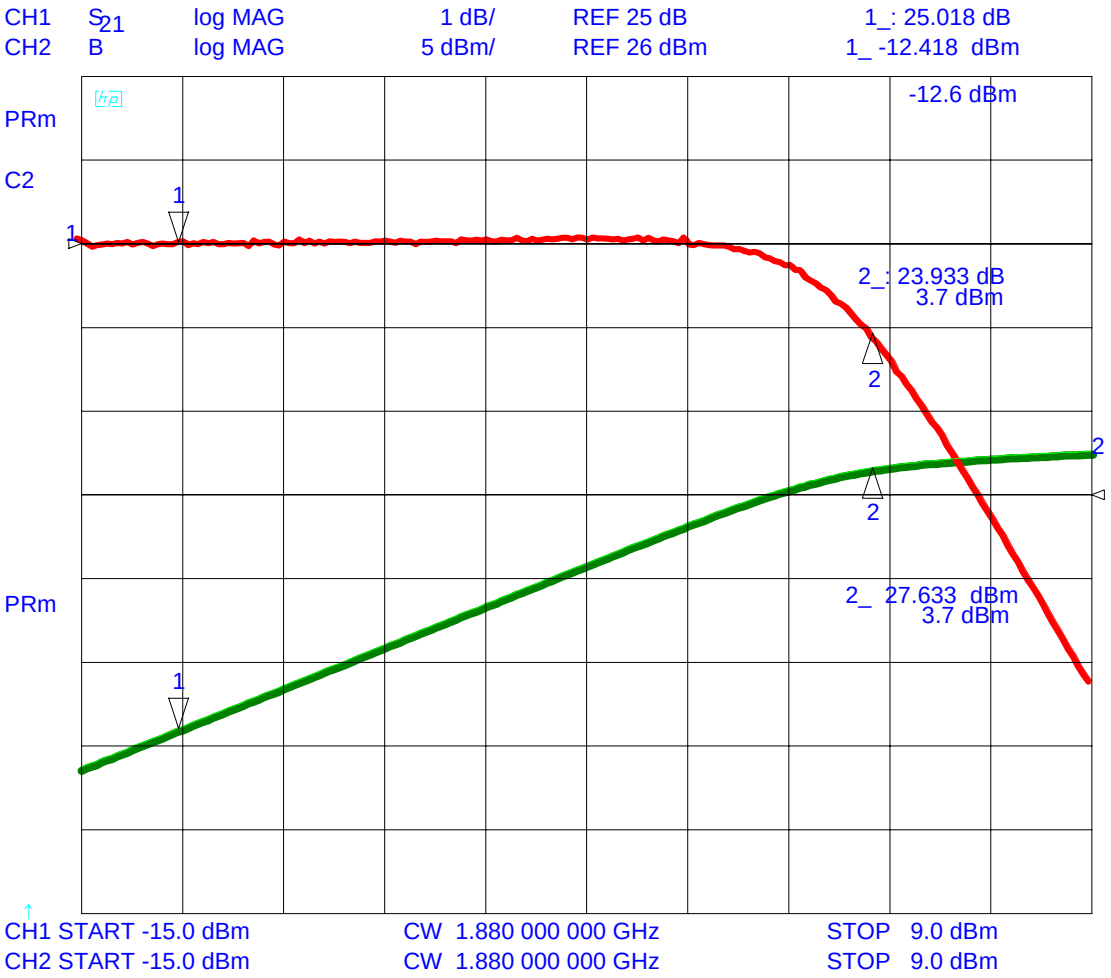




Power Sweep - Compression



Measured Gain Compression



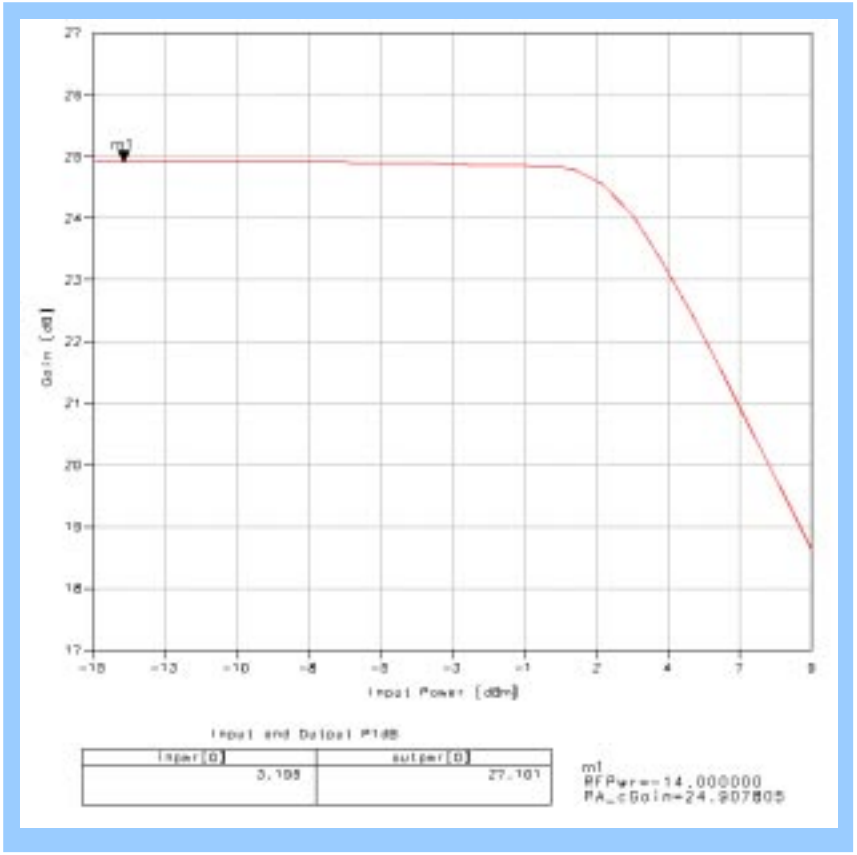
1 dB compression: input power resulting in 1 dB ***drop*** in gain

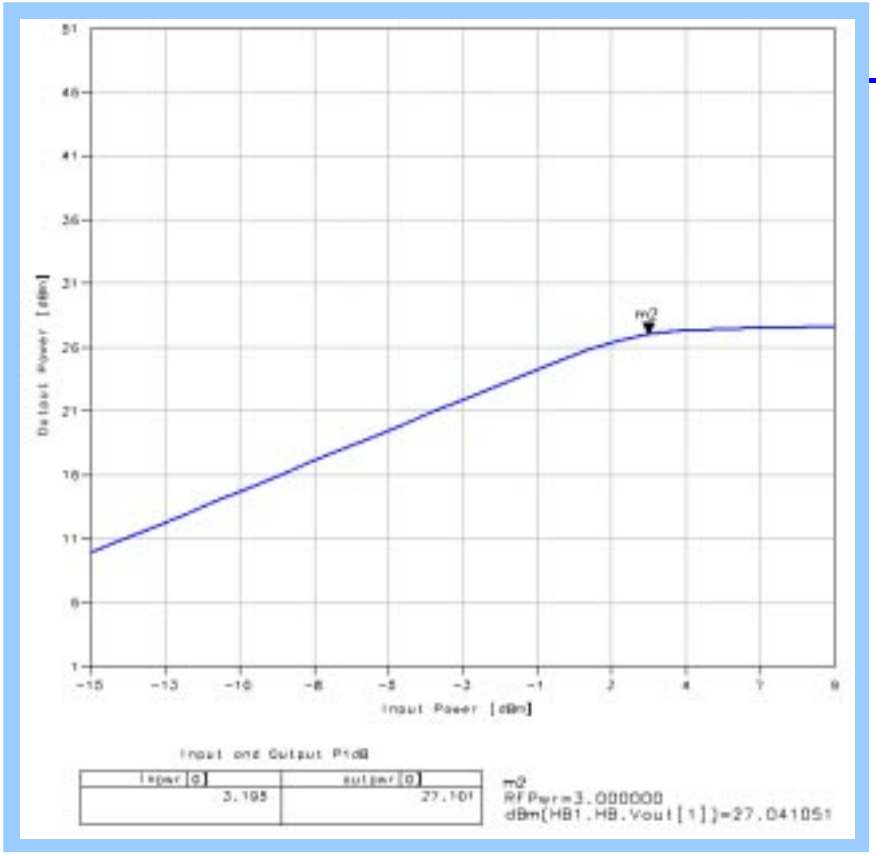
- ratioed measurement
- output power available (non-ratioed measurement)
- use power-meter calibration for best accuracy

1dB Compression Results:
Input power: 3.7 dBm Output power: 27.633 dBm Gain,1dB : 23.933 dB

HEWLETT® PACKARD

Simulated Gain Compression





1dB Compression Results:

Input power: 3.195 dBm **Output power: 27.101 dBm** **Gain, 1dB : 23.907 dB**

HEWLETT® PACKARD

Amplifier Specification Sheet

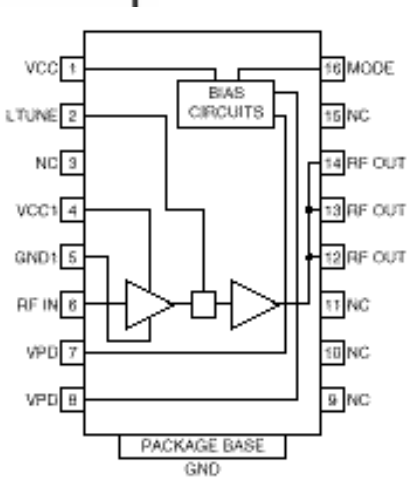
RF MICRO·DEVICES

Preliminary

RF2152

DUAL-MODE CDMA/AMPS OR TDMA/AMPS 3V POWER AMPLIFIER

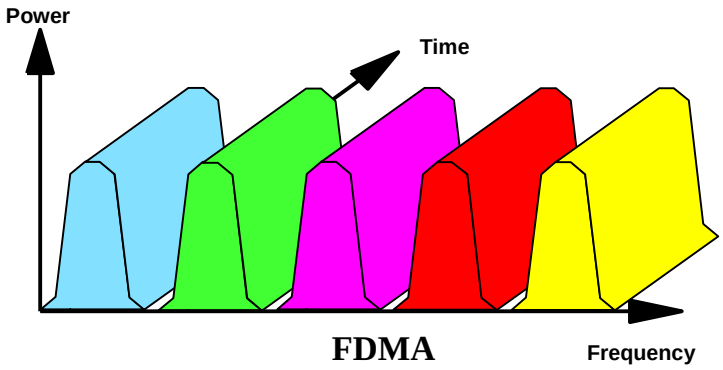
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.5V, Freq=824MHz to 849MHz unless otherwise specified
Usable Frequency Range	800		960	MHz	
Typical Frequency Range		824-849		MHz	
		877-925		MHz	
Linear Gain	28	30	33	dB	Pout=28dBm
Second Harmonic (including second harmonic trap)	-32	-38	-42	dBc	
Max CW Output Power	31	31.5	32	dBm	
Total Efficiency (AMPS mode)	45	50	60	%	
Maximum Linear Output Power (CDMA Modulation)	28	28.5	29	dBm	Tuned for CDMA
Total Linear Efficiency	30	35	38	%	
Adjacent Channel Power Rejection	-44	-46	-50	dBc	ACPR @885kHz
Adjacent Channel Power Rejection	-56	-58	-62	dBc	ACPR @1980kHz
Input VSWR		< 2:1			
Output Load VSWR			10:1		No oscillations

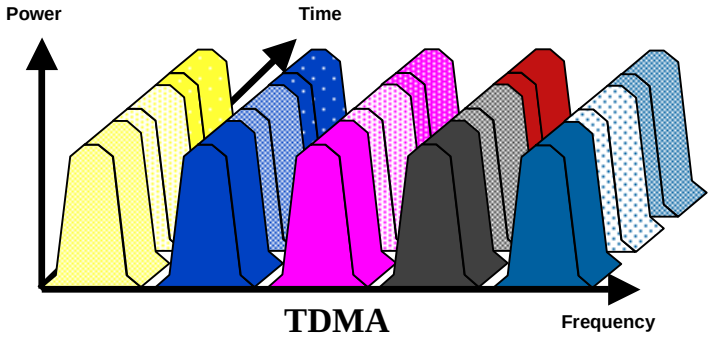


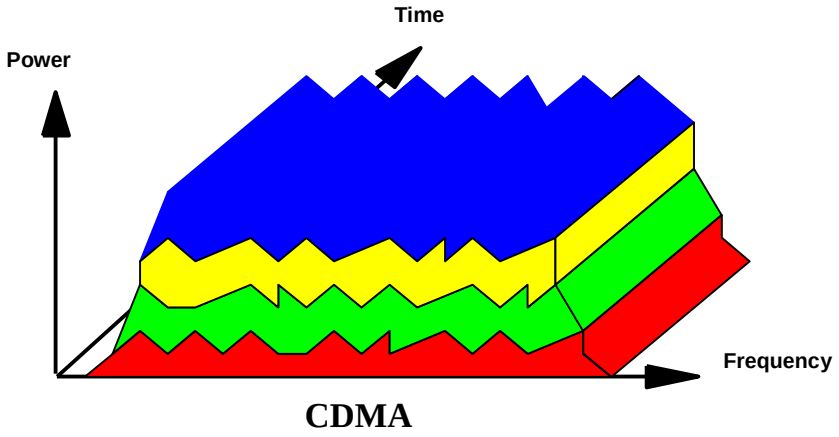
HEWLETT® PACKARD

Digital Modulation Review

Cellular Access Methods



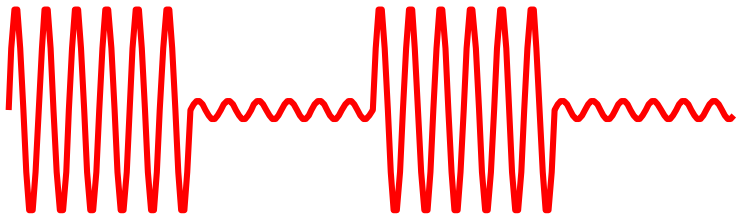




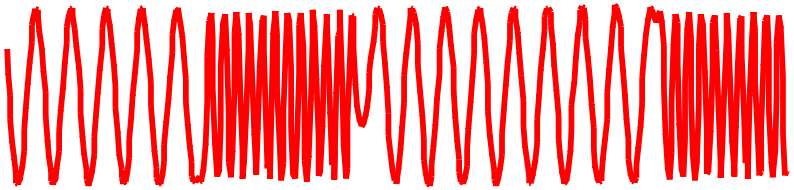
HEWLETT® PACKARD

Digital Modulation Review
…signal characteristics to modulate

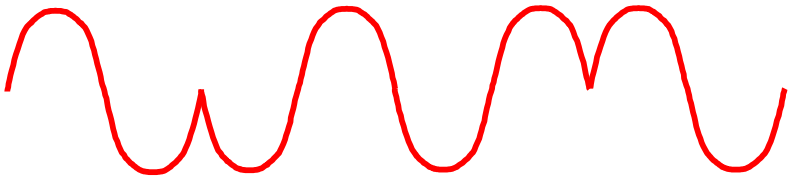
Amplitude



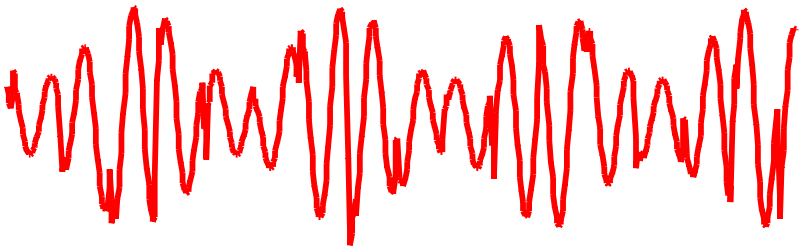
Frequency



Phase

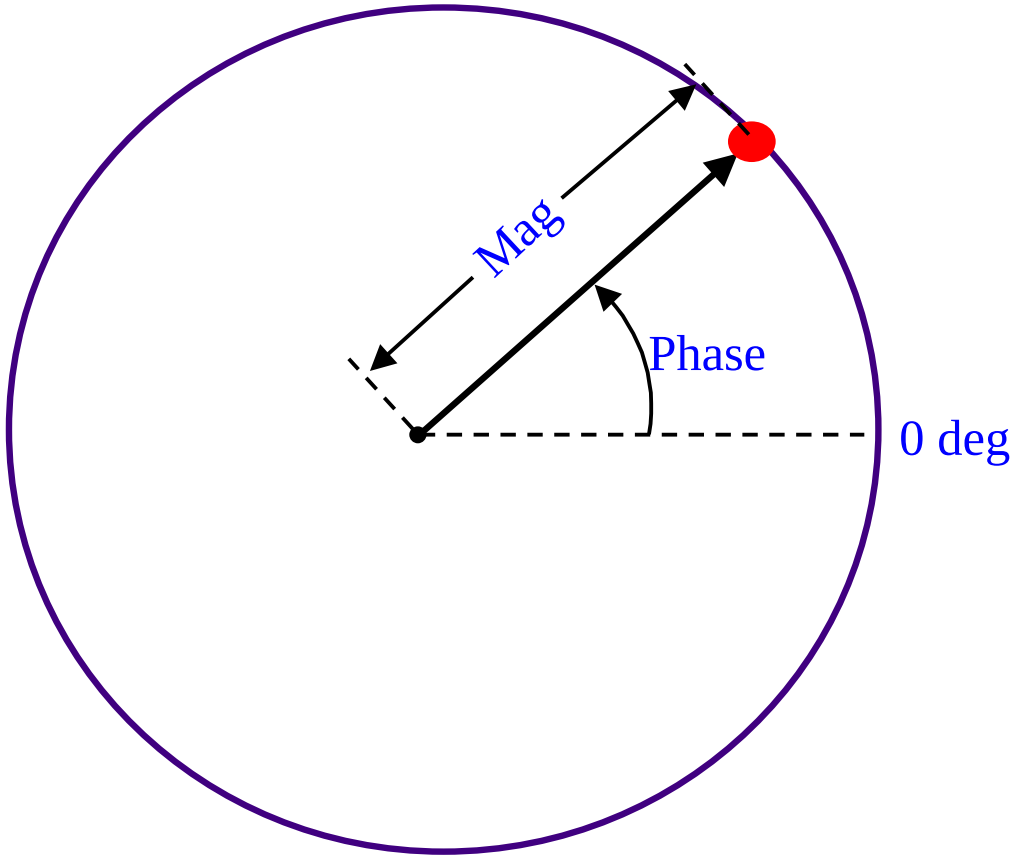


Both Amplitude and Phase



Digital Modulation Review

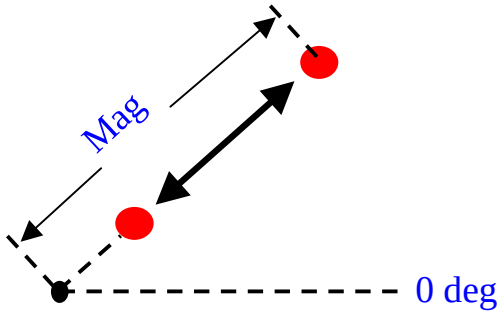
Polar Display: Magnitude & Phase Represented Together



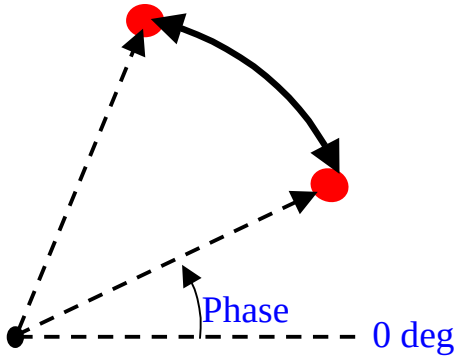
- Magnitude is an absolute value
- Phase is relative to a reference signal

Digital Modulation Review

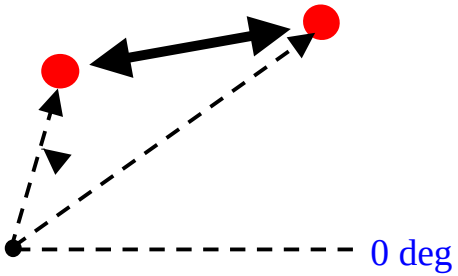
Signal Changes or Modifications



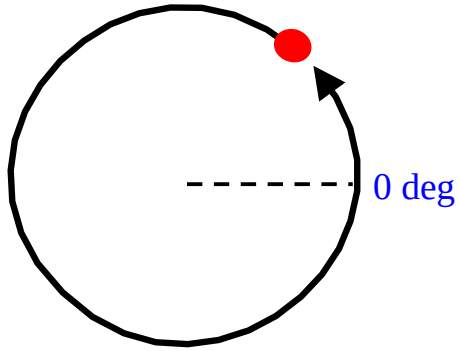
Magnitude Change



Phase Change



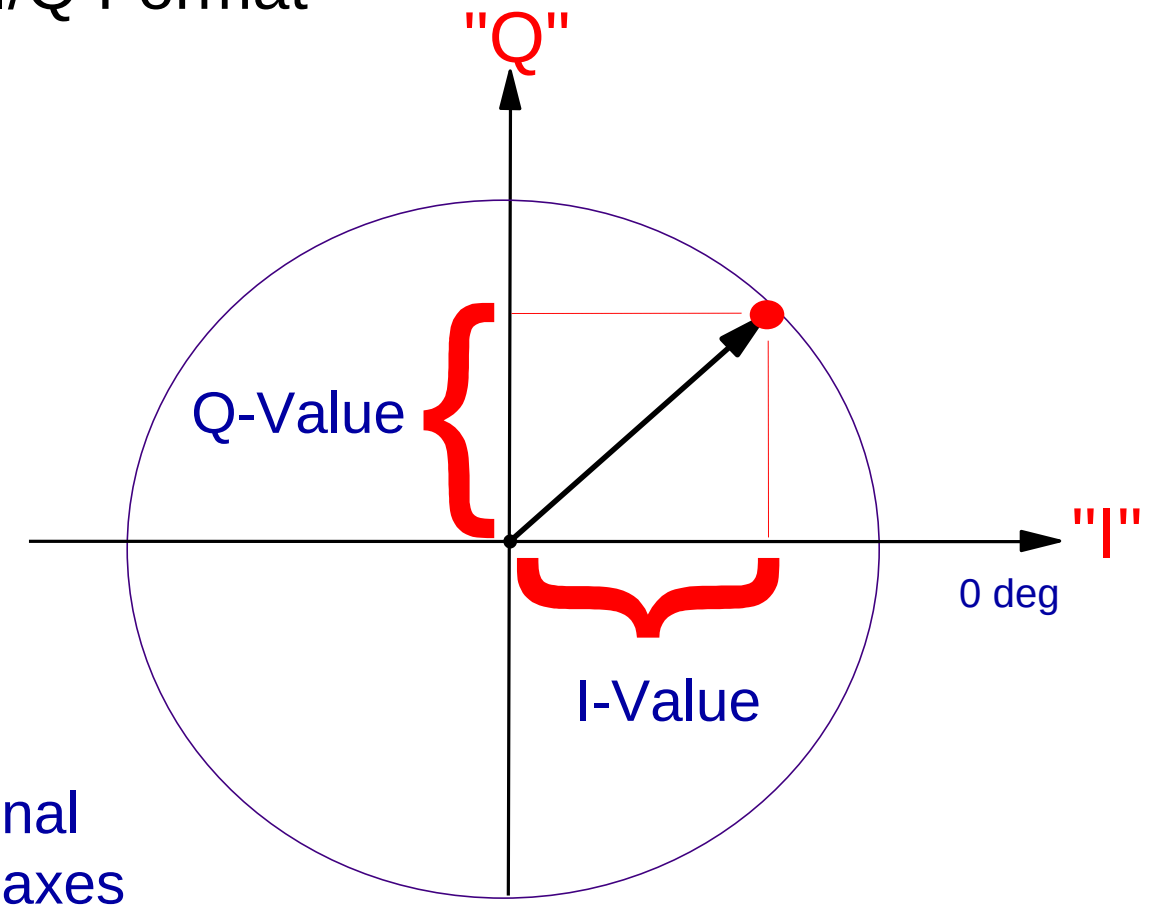
Both Change



Frequency Change

Digital Modulation Review

Polar vs. I/Q Format



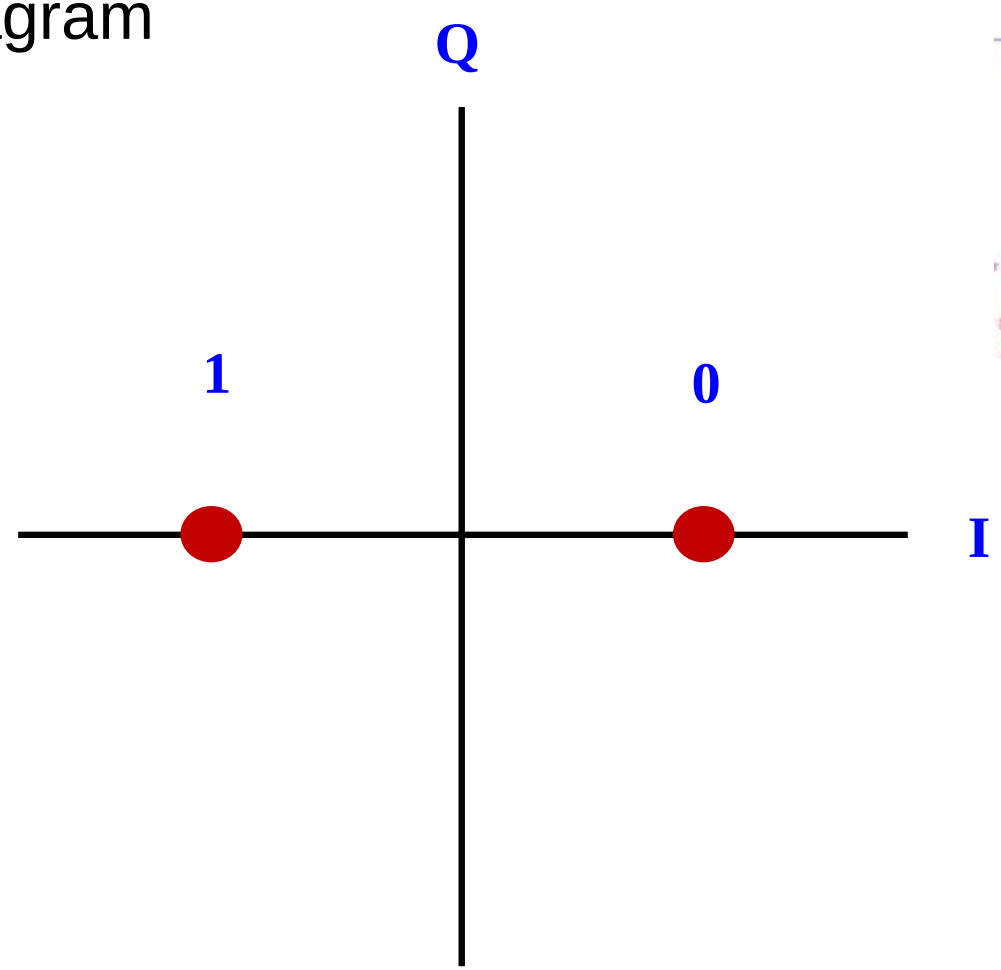
Project signal
to I and Q axes

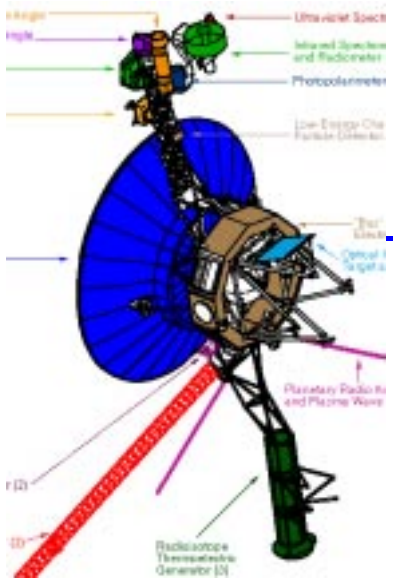
Polar to Rectangular Conversion

Digital Modulation Review

Binary Phase Shift Keying (BPSK)

I/Q Diagram

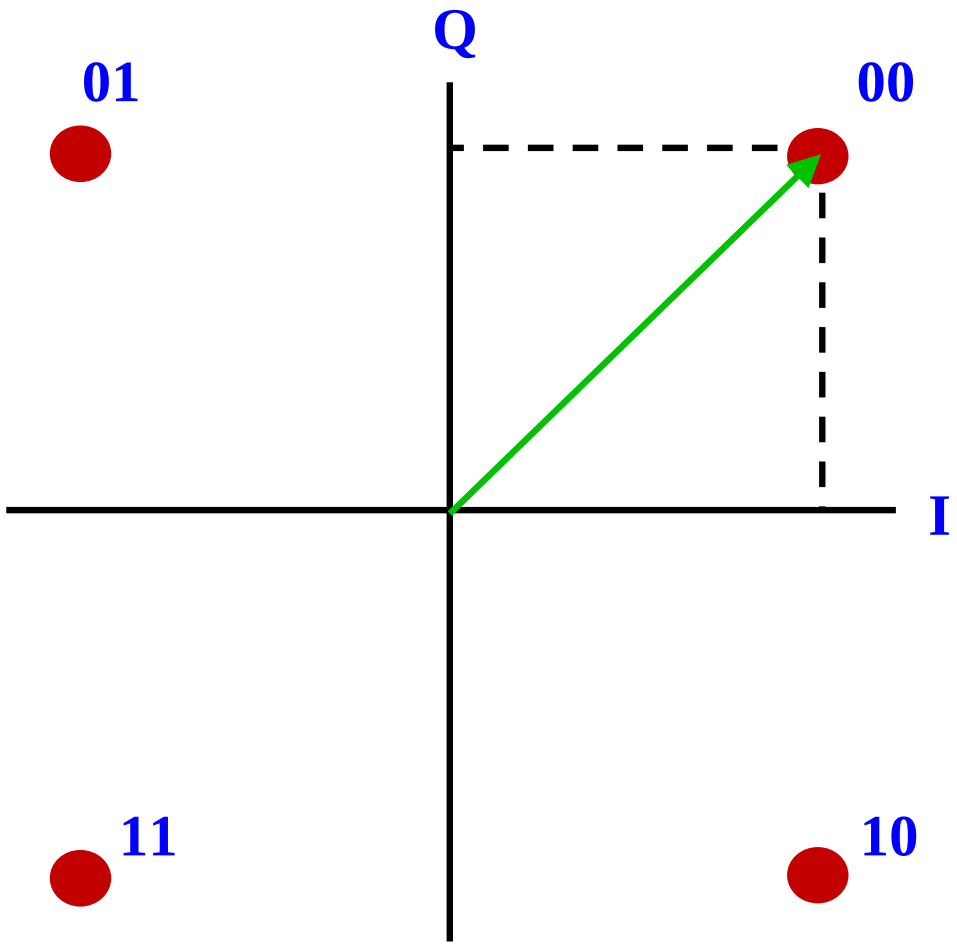




Digital Modulation Review

Quadrature Phase Shift Keying (QPSK)

IQ Diagram

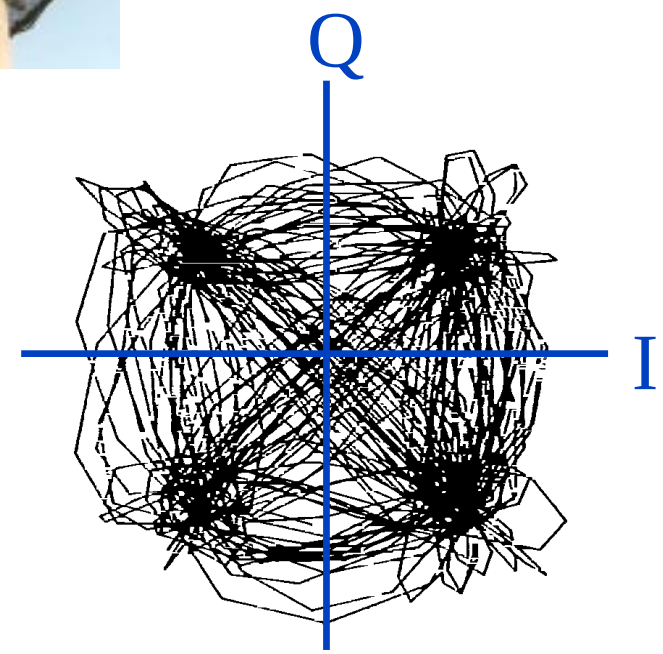


HEWLETT® PACKARD

Digital Modulation Review

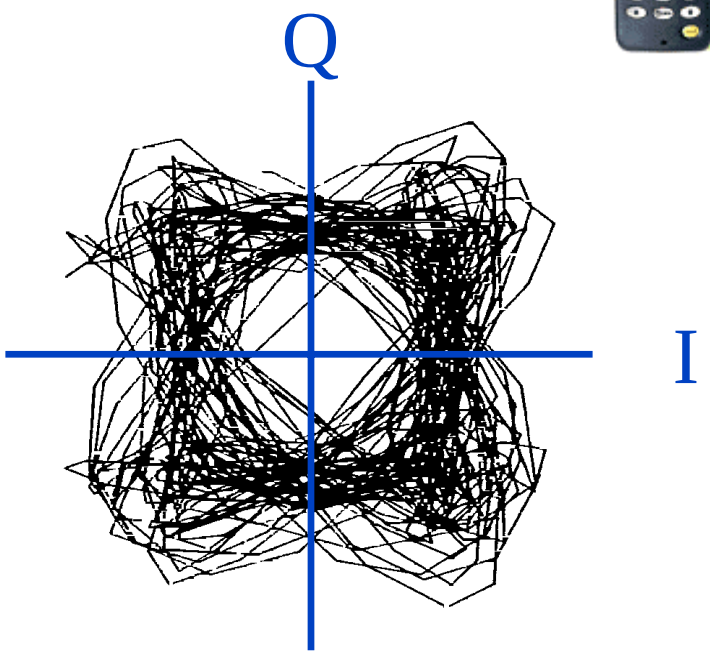
CDMA Modulation Formats

Base Station Transmitter



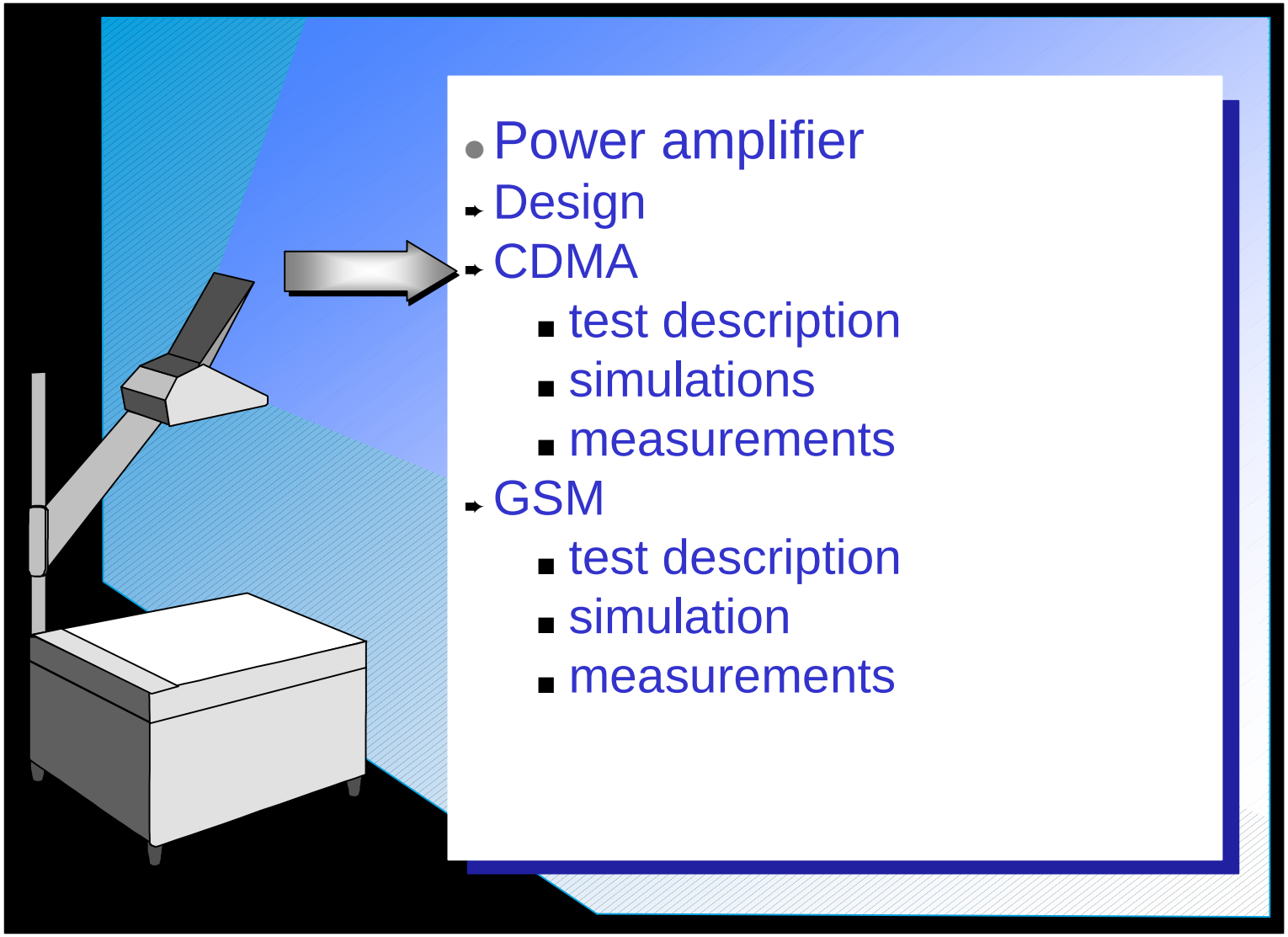
QPSK

Mobile Station Transmitter



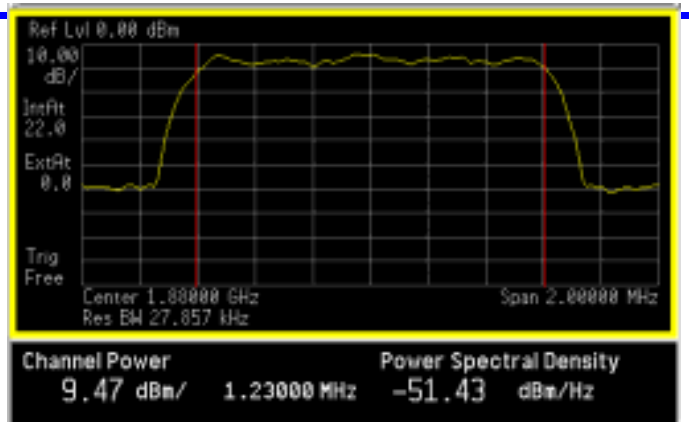
Offset QPSK

Agenda

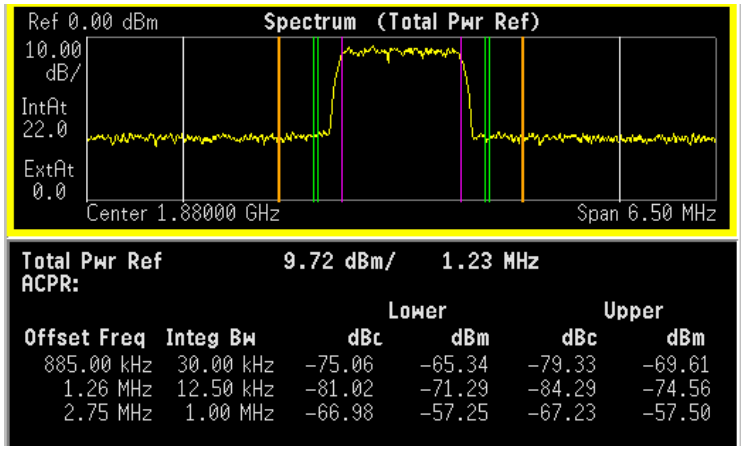


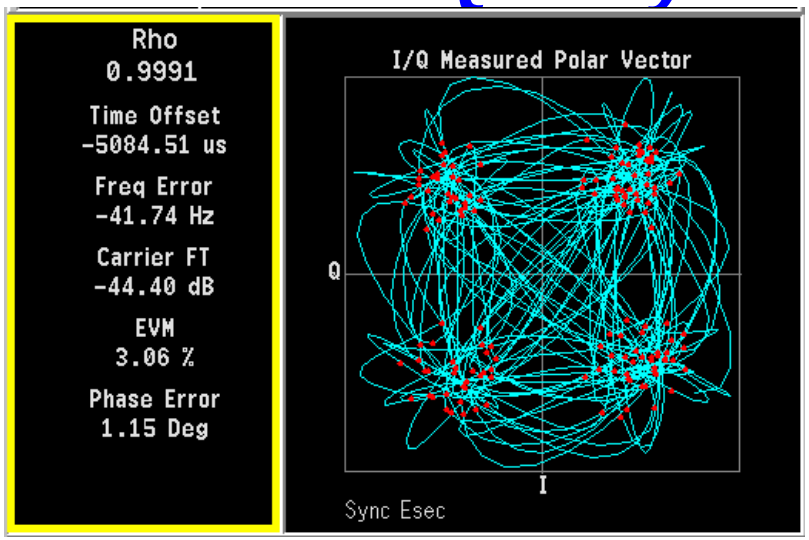
- Power amplifier
- Design
- CDMA
  - test description
  - simulations
  - measurements
- GSM
  - test description
  - simulation
  - measurements

CDMA Tests



- ***Channel Power***
- ***Adjacent Channel Power Ratio (ACPR)***
- ***Modulation Quality***

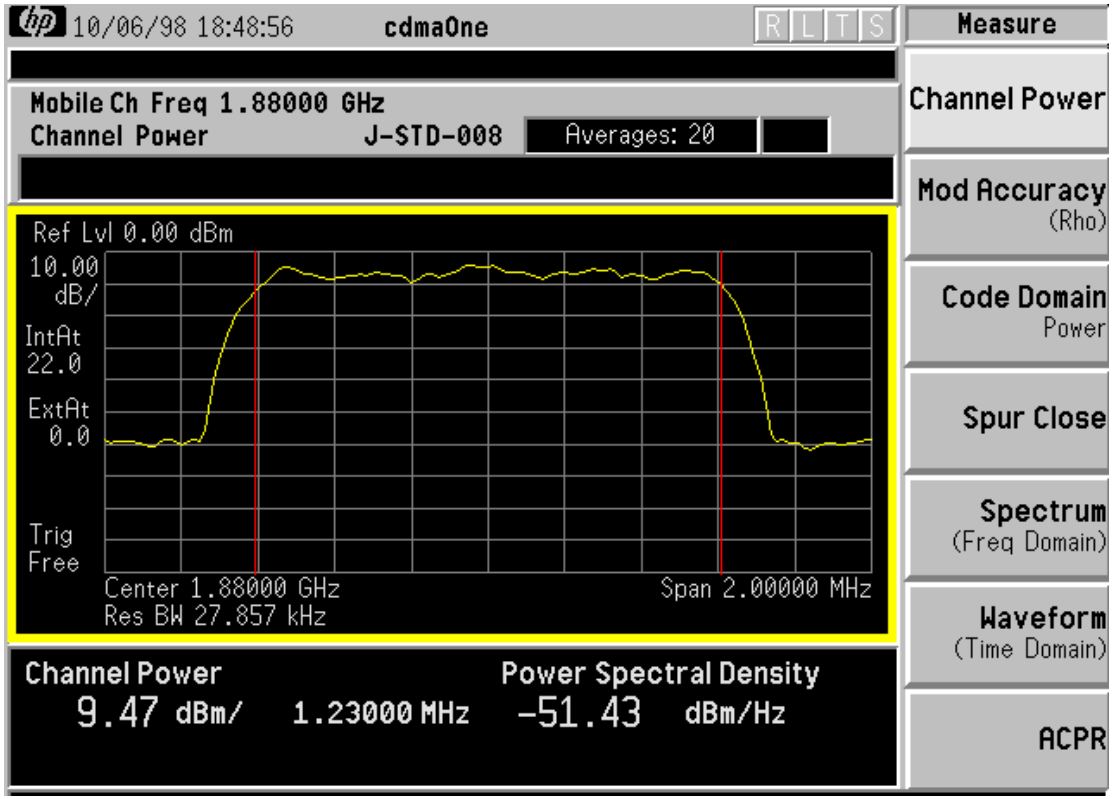




HEWLETT® PACKARD

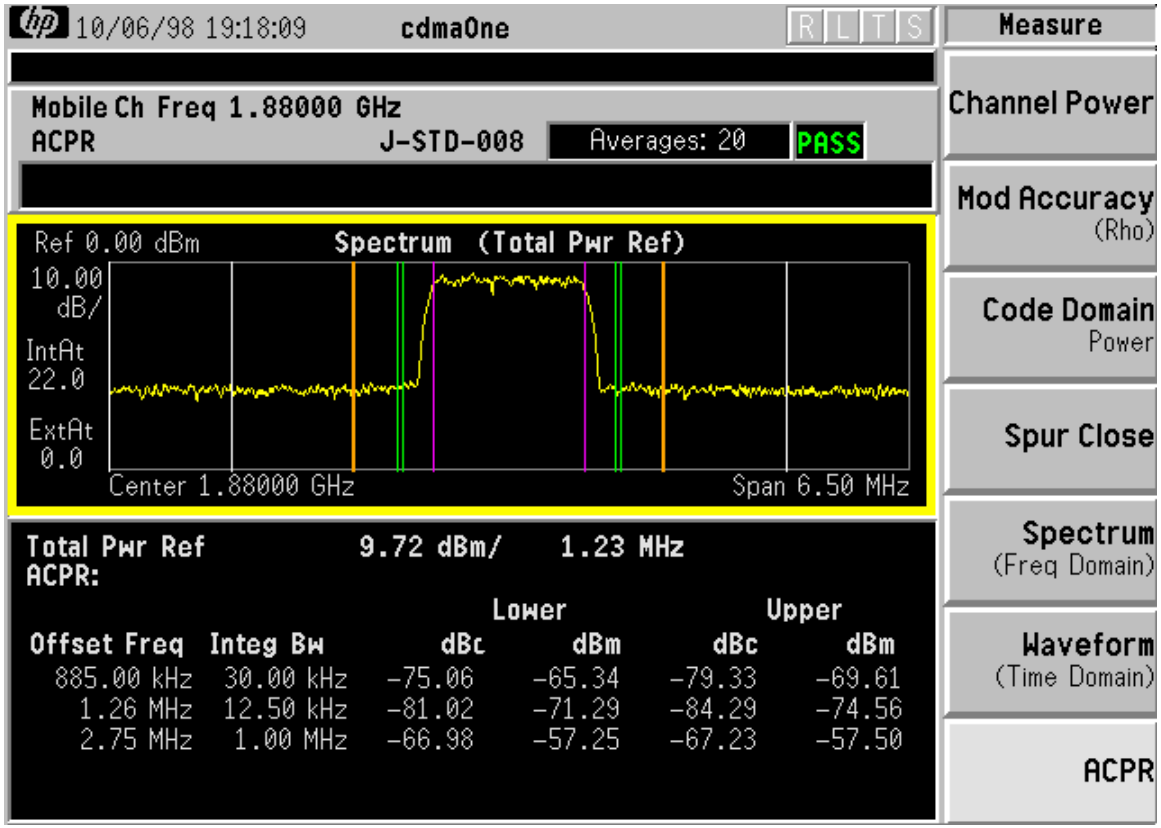
CDMA Tests

Channel Power is band limited to 1.23 MHz



CDMA Tests

ACPR compares in-channel power to out-of-channel power



HEWLETT® PACKARD

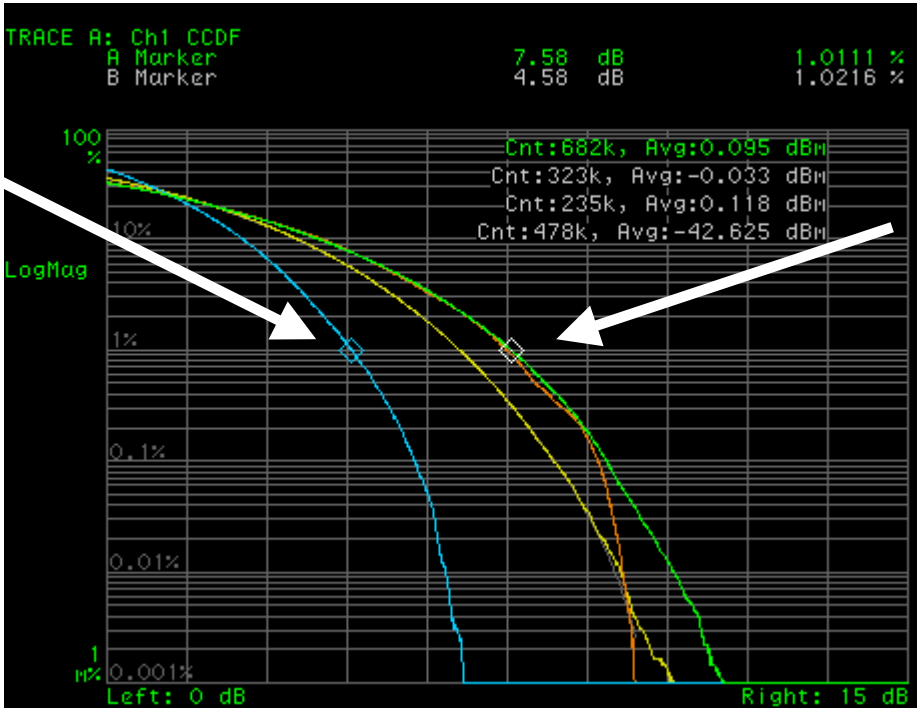
Base Station Spec <-45 dBc @ 885 KHz

CDMA Tests

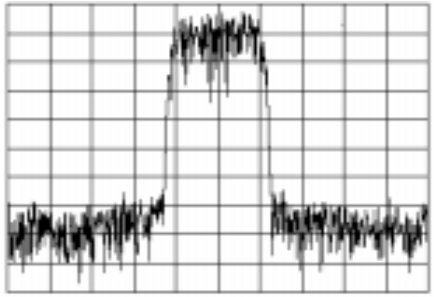
HP E4433B ESG Generator

What's CCDF?

Less stressful



More stressful

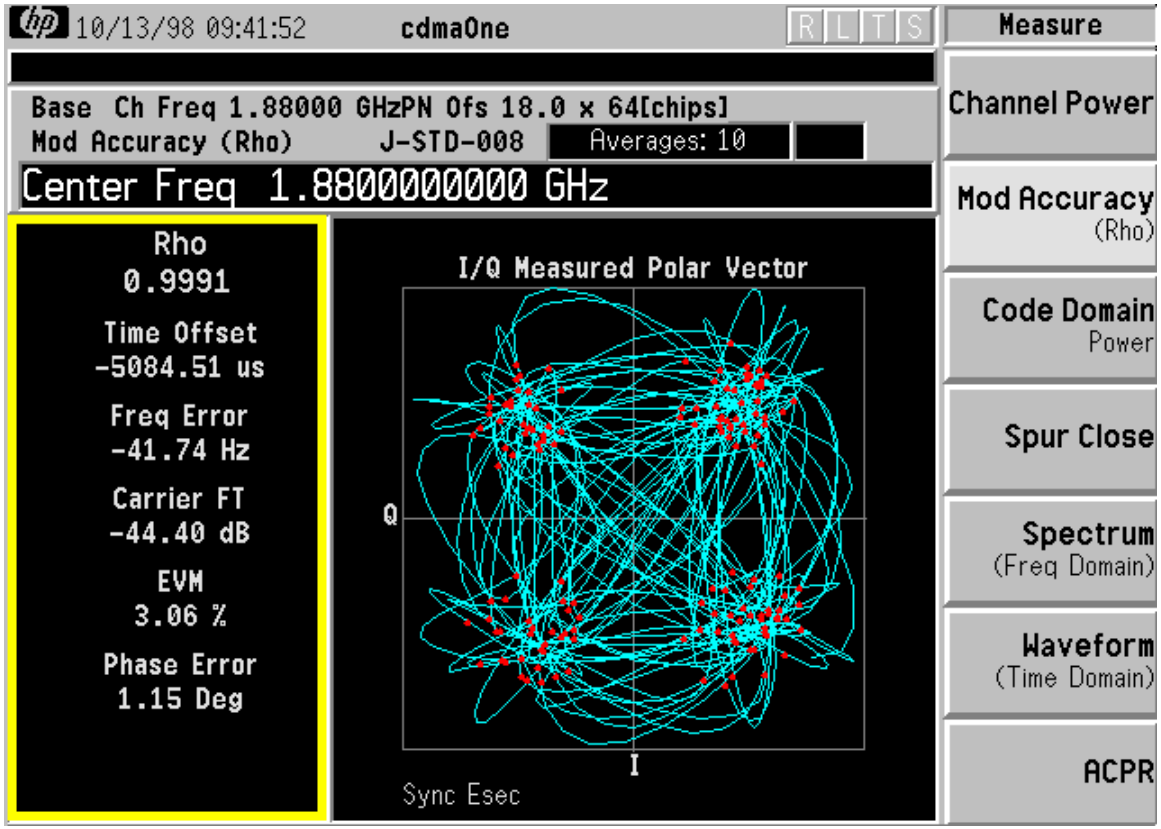


Assures adequate test signal for ACPR

HEWLETT® PACKARD

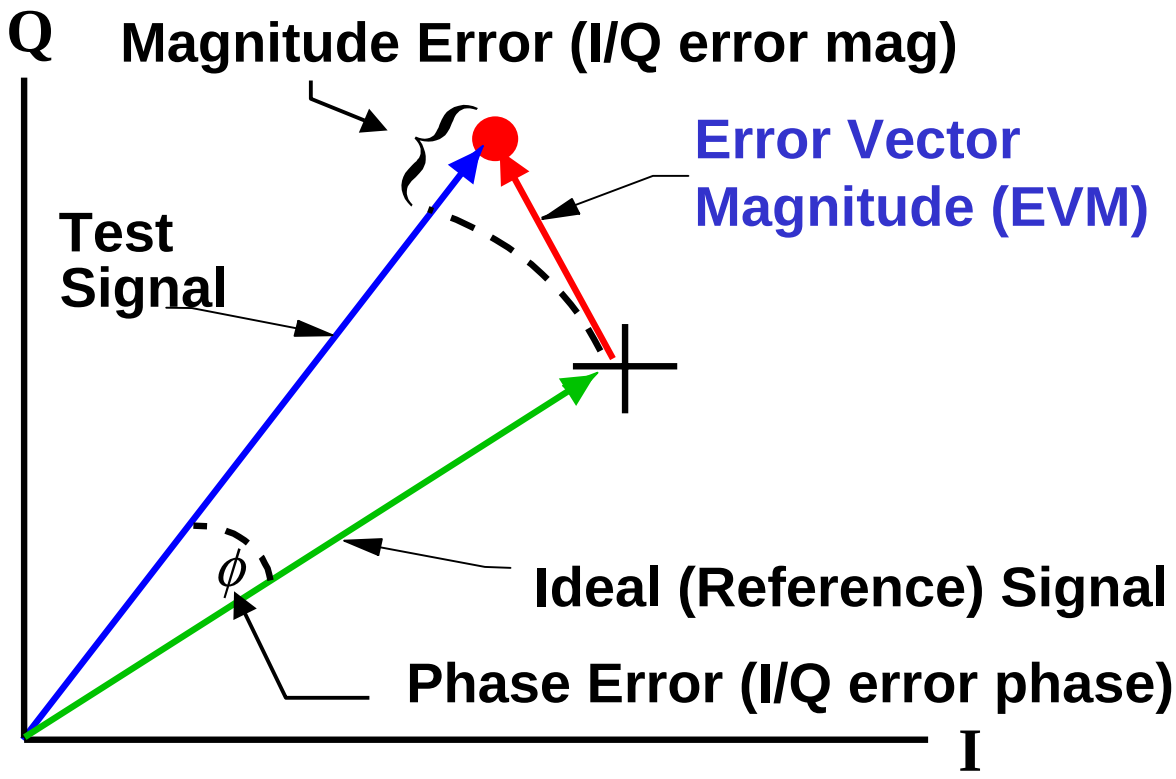
CDMA Tests

Modulation Quality (EVM & Rho)



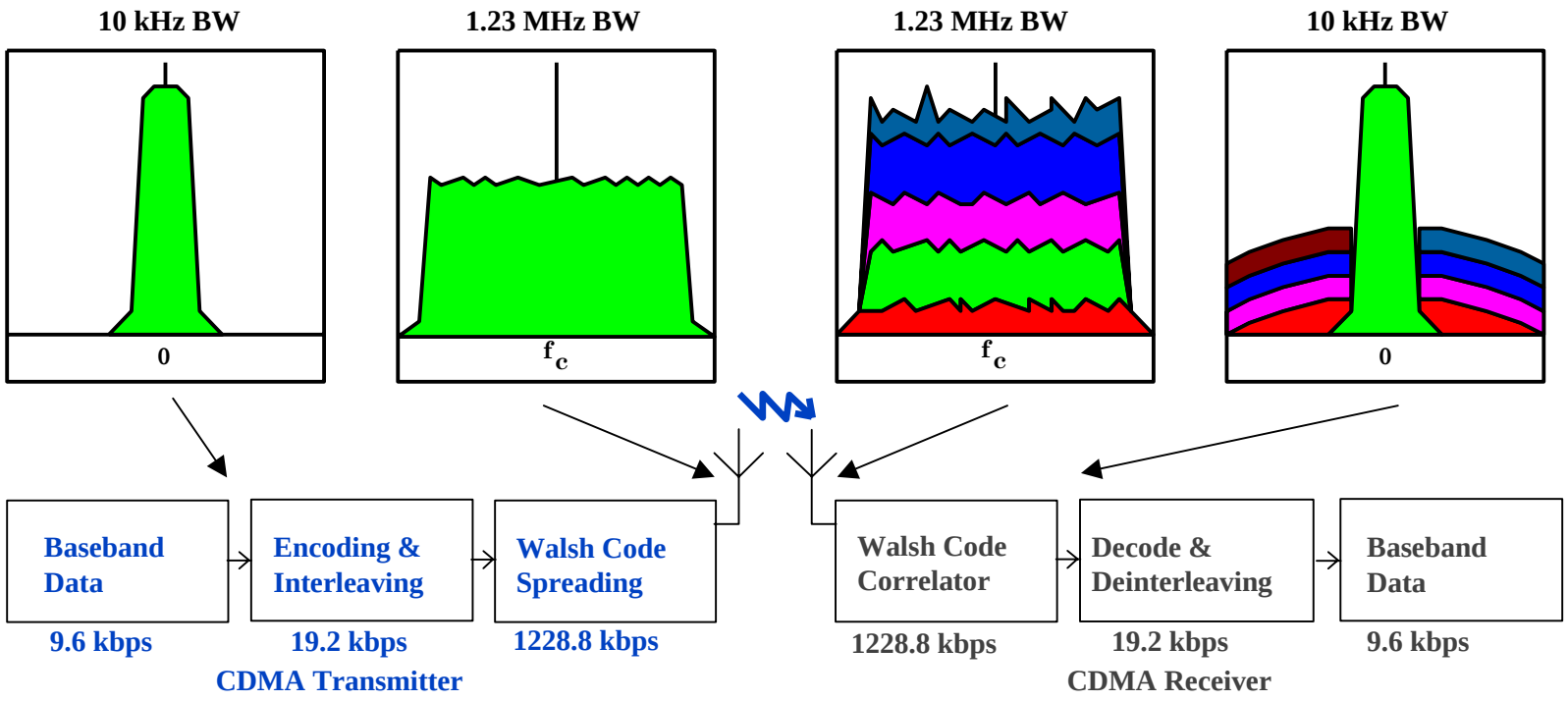
HEWLETT® PACKARD

What's EVM?



… EVM is the RMS value of the error vector.

What's Rho?



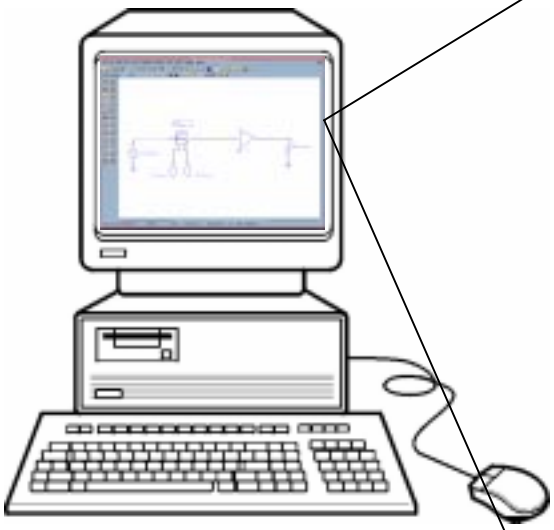
If data is "spread and de-spread" perfectly, Rho=1

Base Station Spec >.912, Mobile >.944

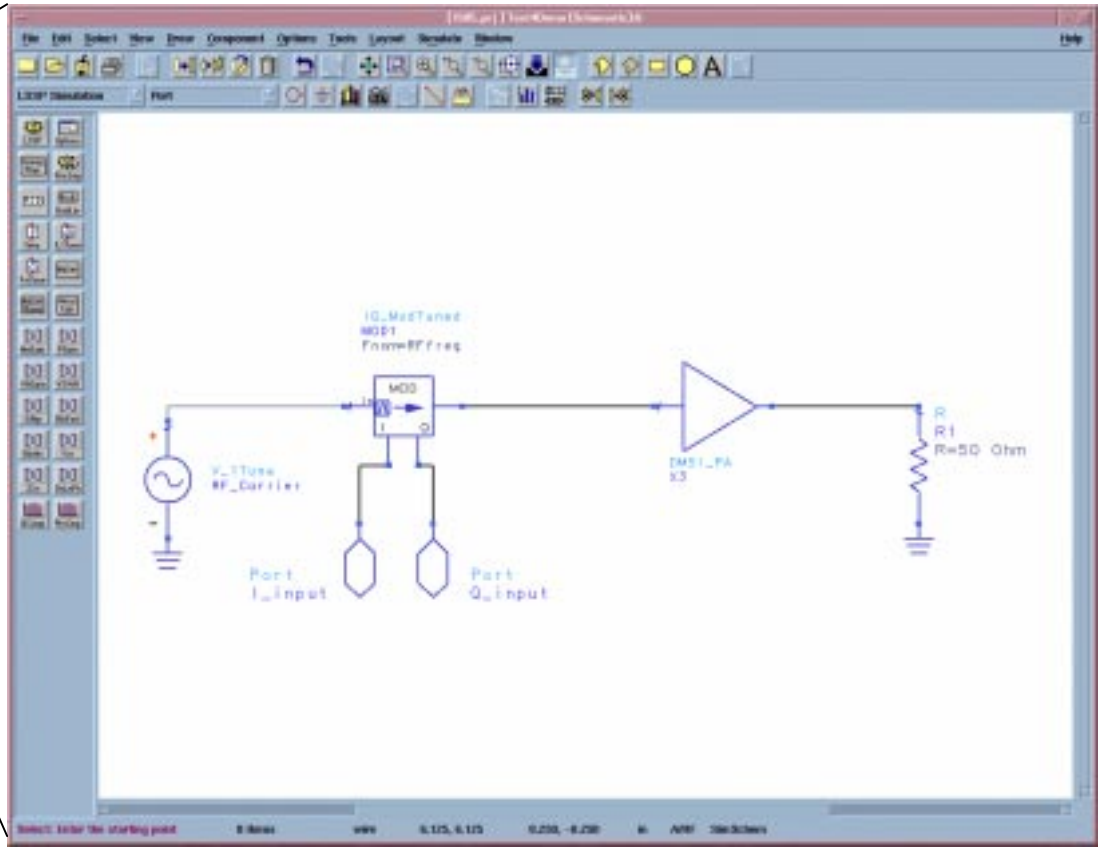
HEWLETT® PACKARD

CDMA Tests

Simulation Setup



HP Advanced Design System

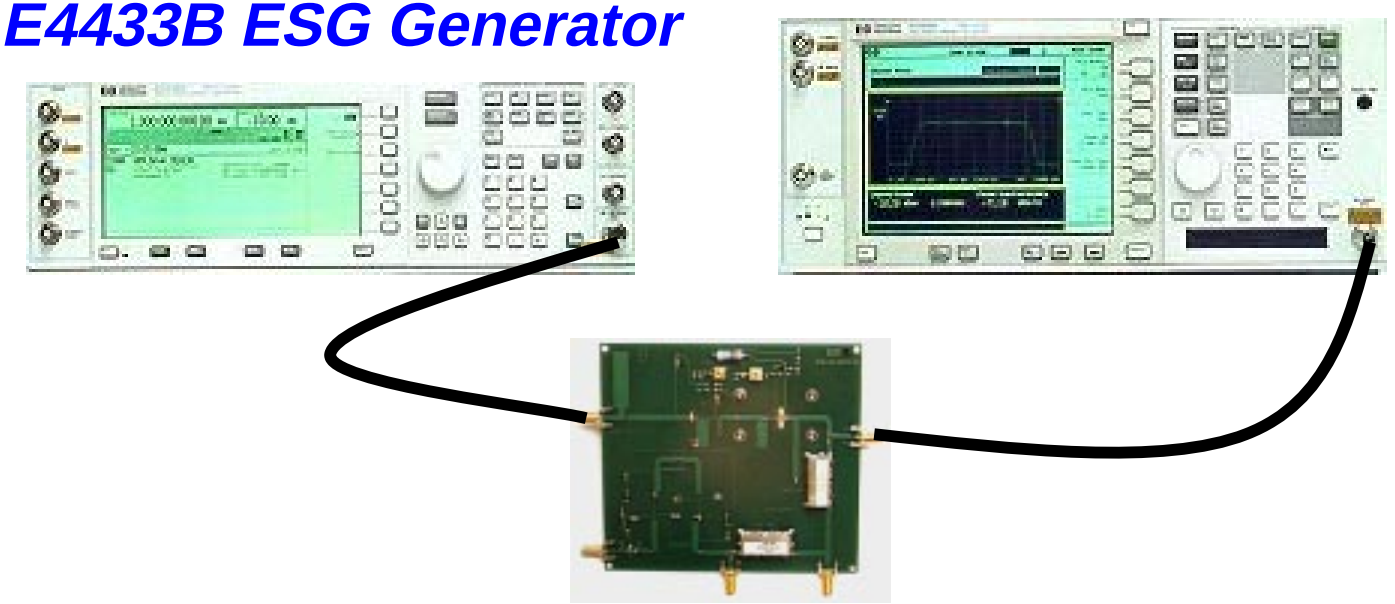


CDMA Tests

Measurement set-up

HP E4433B ESG Generator

HP E4406A VSA Analyzer

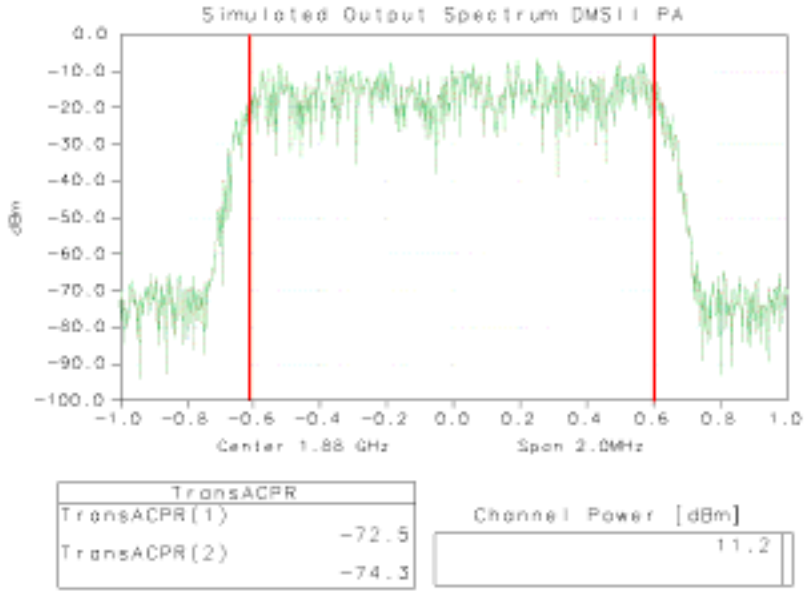


HEWLETT® PACKARD

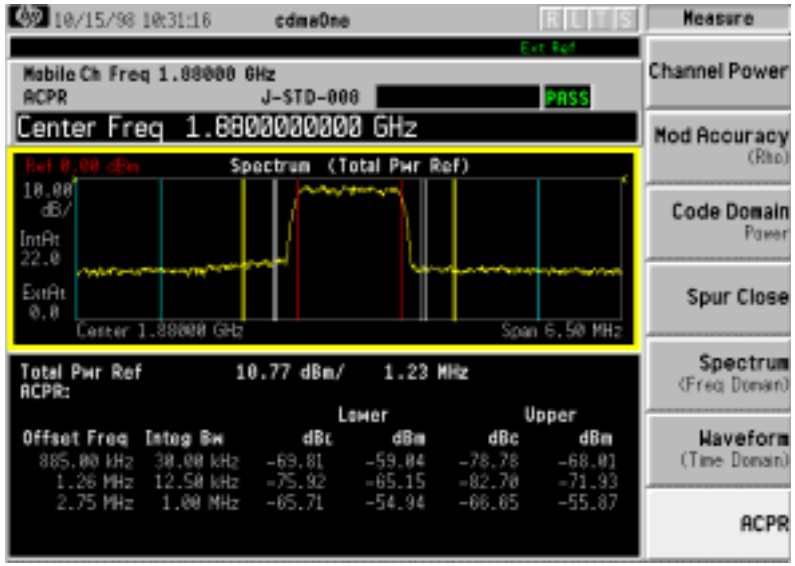
CDMA Tests

Channel Power and ACPR

Simulation



Measured



Pwr = 11.2 dBm
ACPR < -70 dBc

Pwr = 10.8 dBm
ACPR < -70 dBc

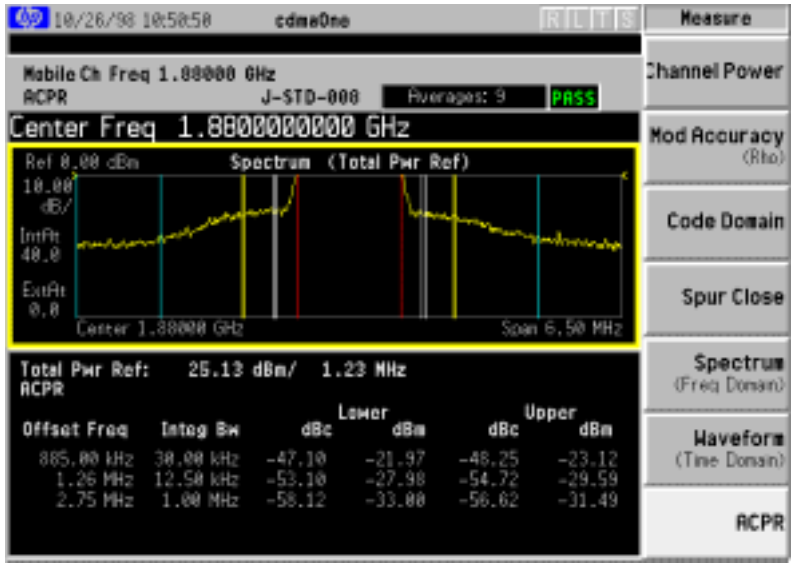
HEWLETT® PACKARD

CDMA Tests

Channel Power and ACPR in Saturation

Simulation

Measured



Pwr = 23.7 dBm
ACPR < -47 dBc

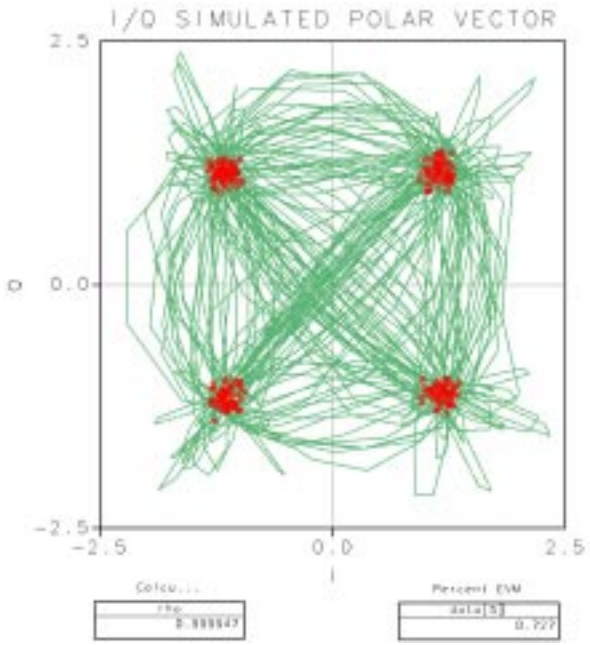
Pwr = 23.2 dBm
ACPR < -47 dBc

HEWLETT® PACKARD

CDMA Tests

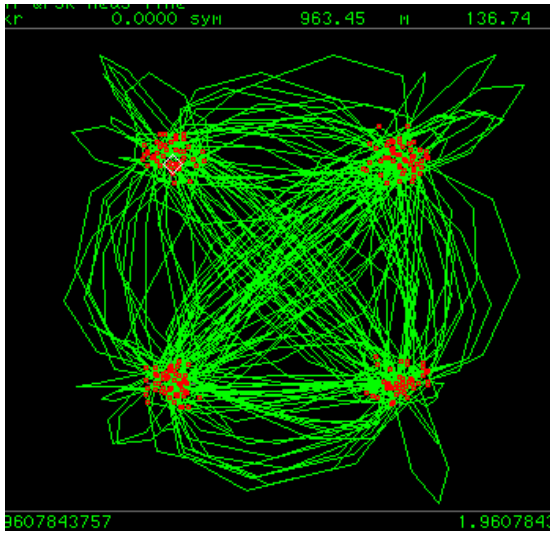
EVM and Rho - No Saturation

Simulation



EVM = .7%
Rho = .999

Measured



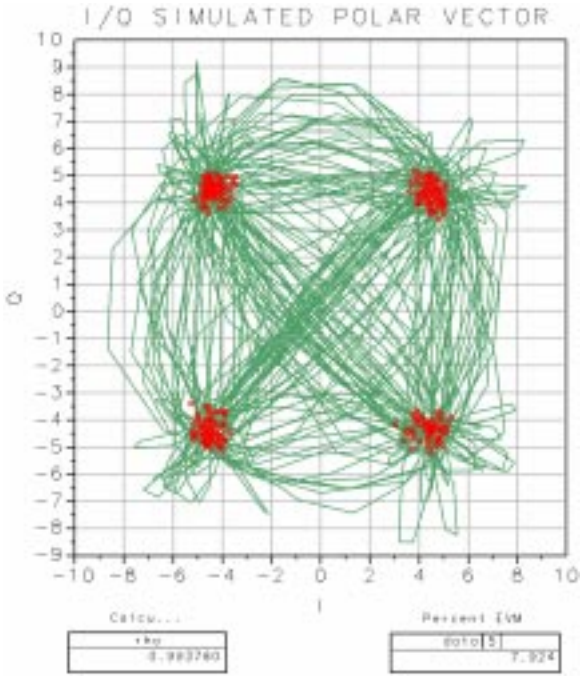
EVM = 1.5%
Rho = .999

HEWLETT® PACKARD

CDMA Tests

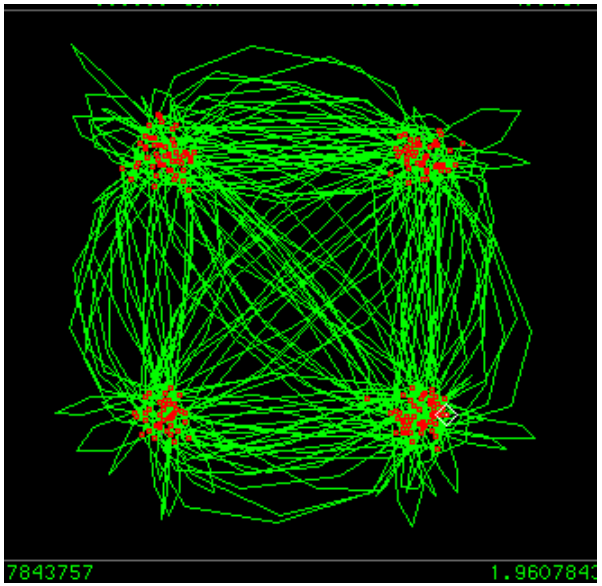
EVM and Rho In Saturation

Simulation



EVM = 8%
Rho = .994

Measured

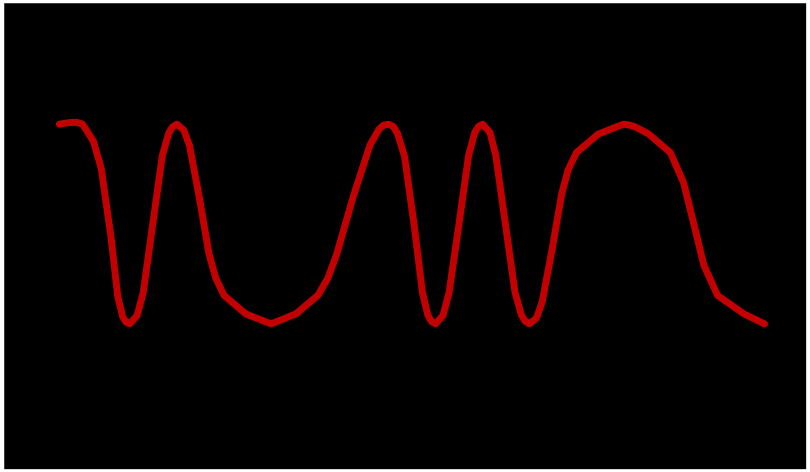


EVM = 5%
Rho = .997

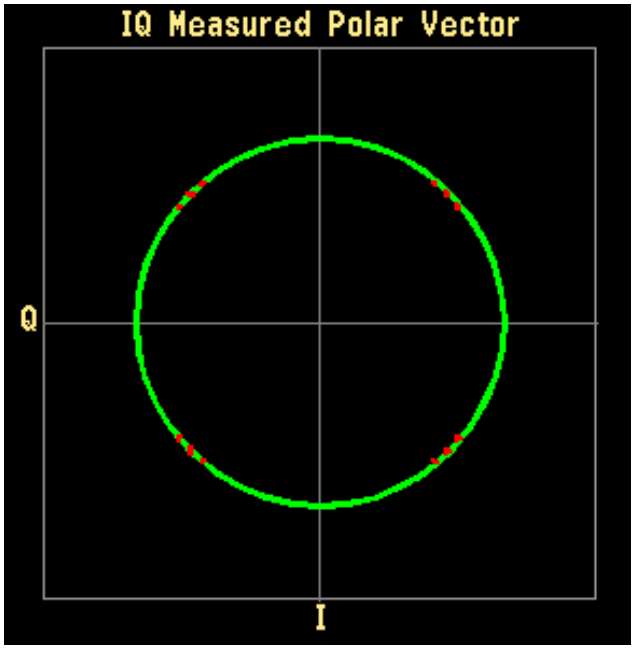
HEWLETT® PACKARD

FSK Modulation Review

Frequency Shift Keying (FSK) Used in Paging



Minimum Shift Keying (MSK) Used in GSM



HEWLETT® PACKARD

GSM Amplifier Specification Sheet

CELERITEK

CMM0335

Advanced Product Information
September 1996 *(1 of 2)*

890 to 915 MHz 6V, 35 dBm, GSM Power Amplifier

Electrical Characteristics

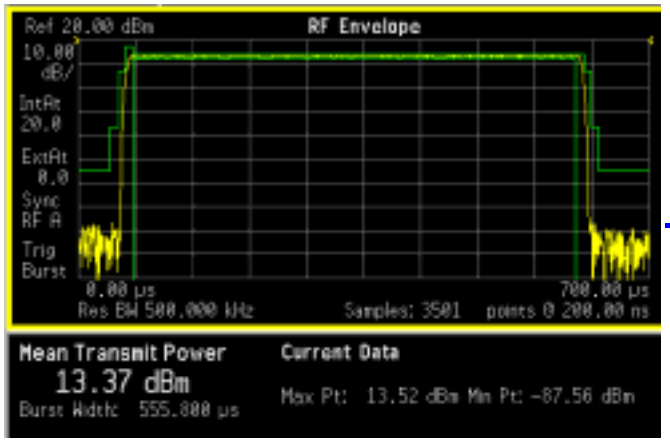
Unless otherwise specified the following specifications are guaranteed at room temperature with drain voltage ($+V_d$) = 5.8 V and P_{IN} = +8 dBm, in Celeritek test fixture.

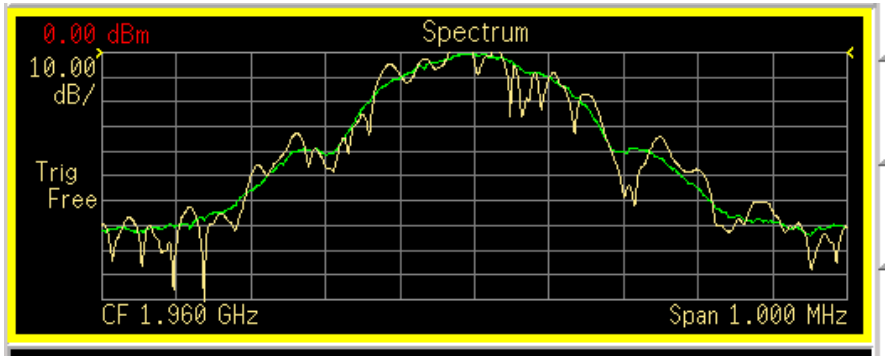
Parameter	Condition	Min	Typ	Max	Units
Frequency Range		890		915	MHz
Pout	PIN = +8 dBm	34.5	35.5		dBm
Efficiency	35 dBm output meeting GSM template	50	55		%
Gain		30	34		dB
Harmonics	2nd @ Pout = +34.5 dBm 3rd @ Pout = +34.5 dBm			-30 -30	dBc dBc
Return Loss	In Celeritek test fixture		10		dB
Negative Supply Current				3	mA
Supply Current			950		mA
Quiescent Current	No RF		250		mA

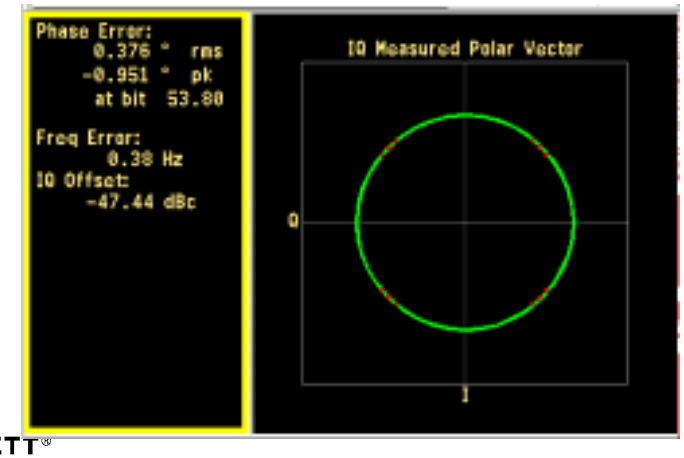
HEWLETT® PACKARD

GSM Tests

- ***Power Vs. Time***
- ***Output RF Spectrum***
- ***Phase and Freq. Error***



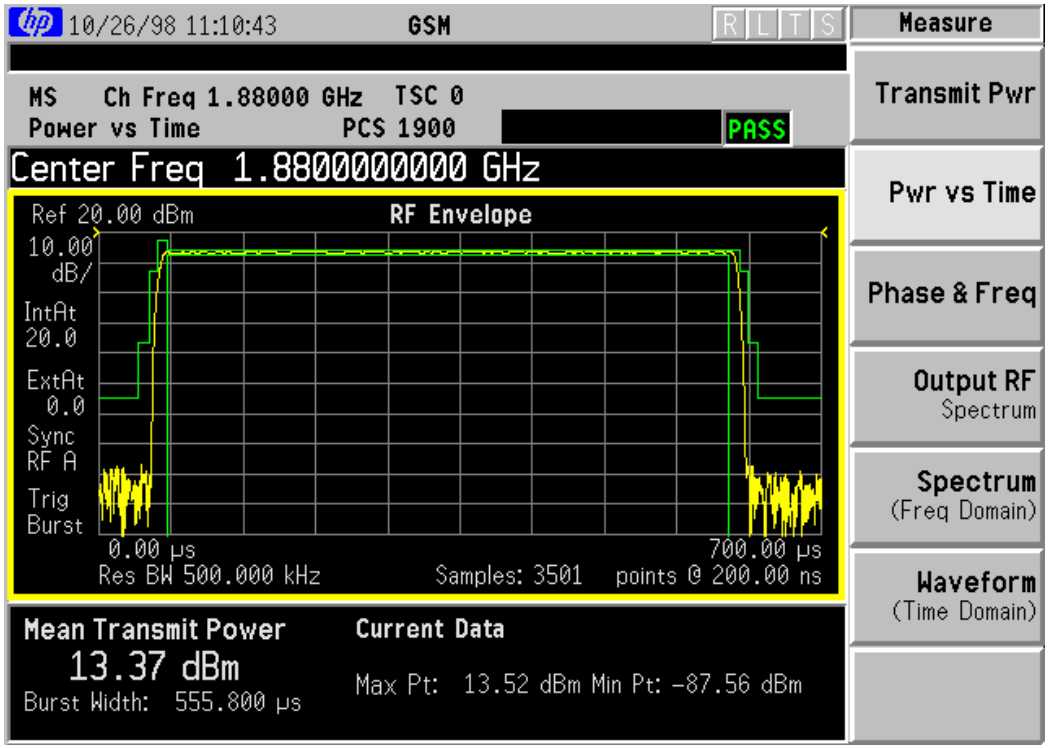




HEWLETT PACKARD

GSM Tests

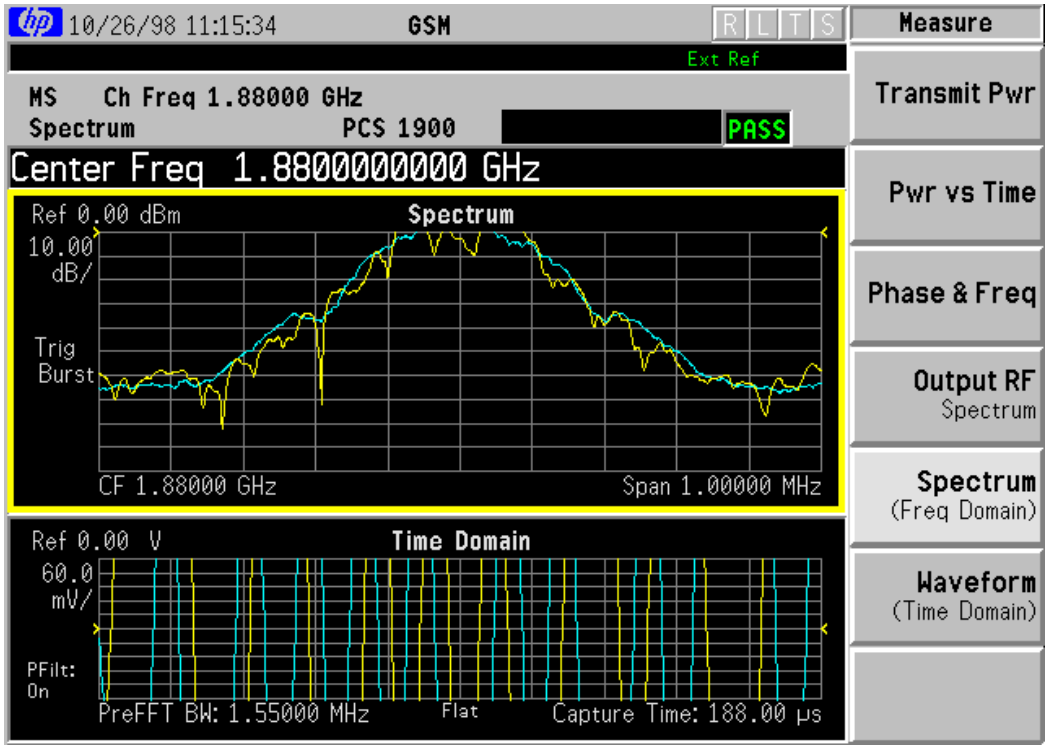
Power vs. Time Measurements Verify Flatness and Timing of the RF Burst.



HEWLETT® PACKARD

GSM Tests

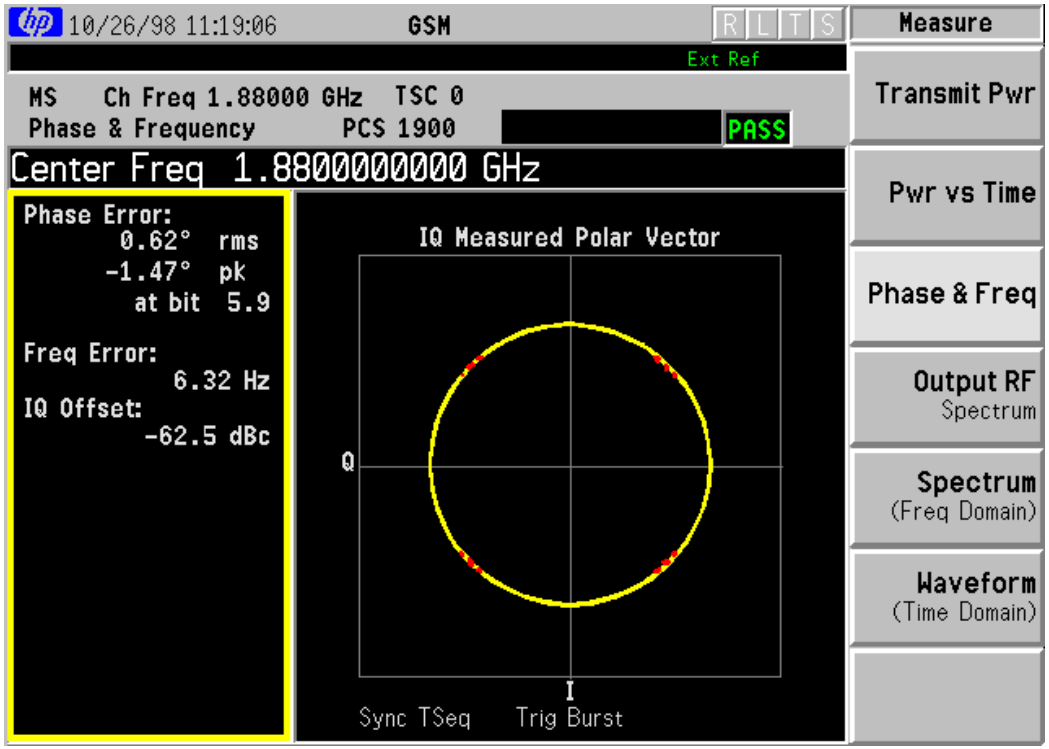
Output RF Spectrum Measurements
Examine Adjacent Channel Interference



HEWLETT® PACKARD

GSM Tests

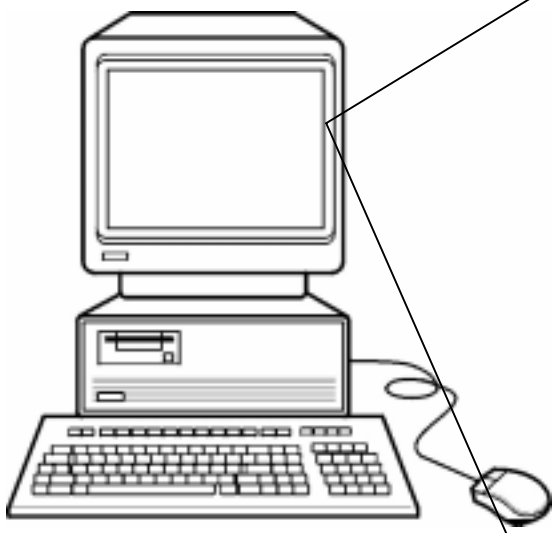
Phase and Frequency Error Determine the Quality of Modulation



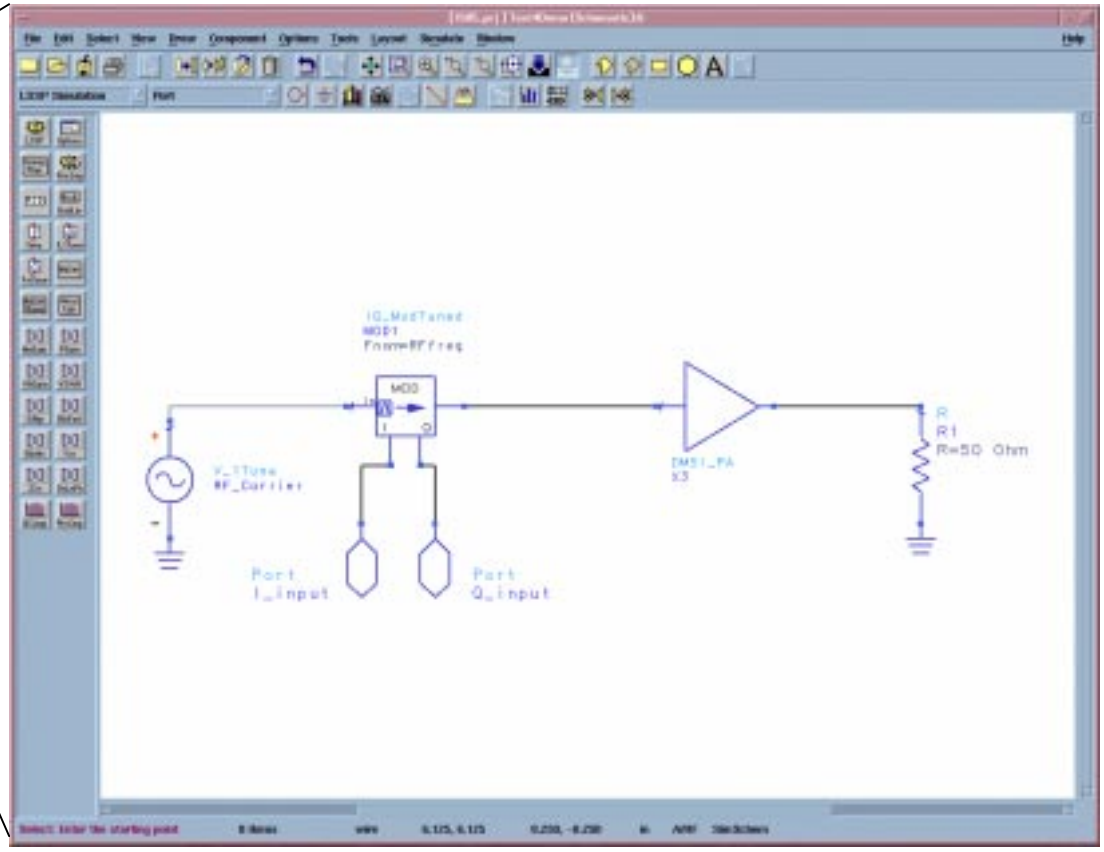
HEWLETT® PACKARD

GSM Tests

Simulation Setup



HP Advanced Design System

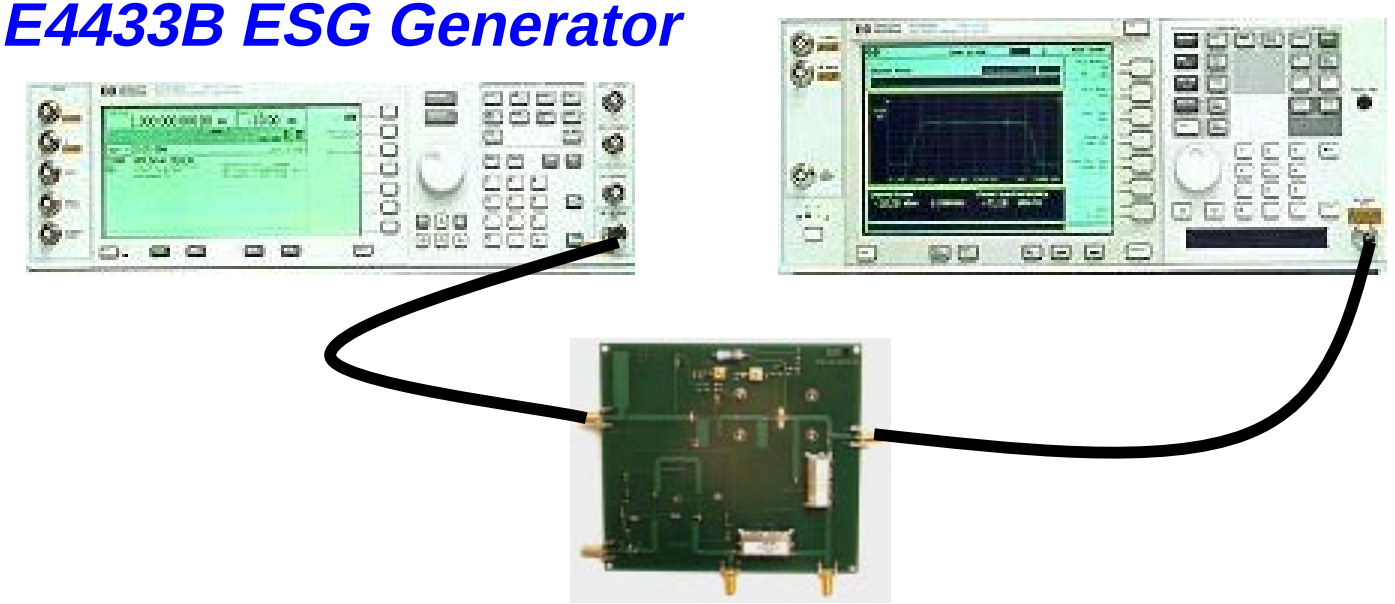


GSM Tests

Measurement Setup

HP E4433B ESG Generator

HP E4406A VSA Analyzer

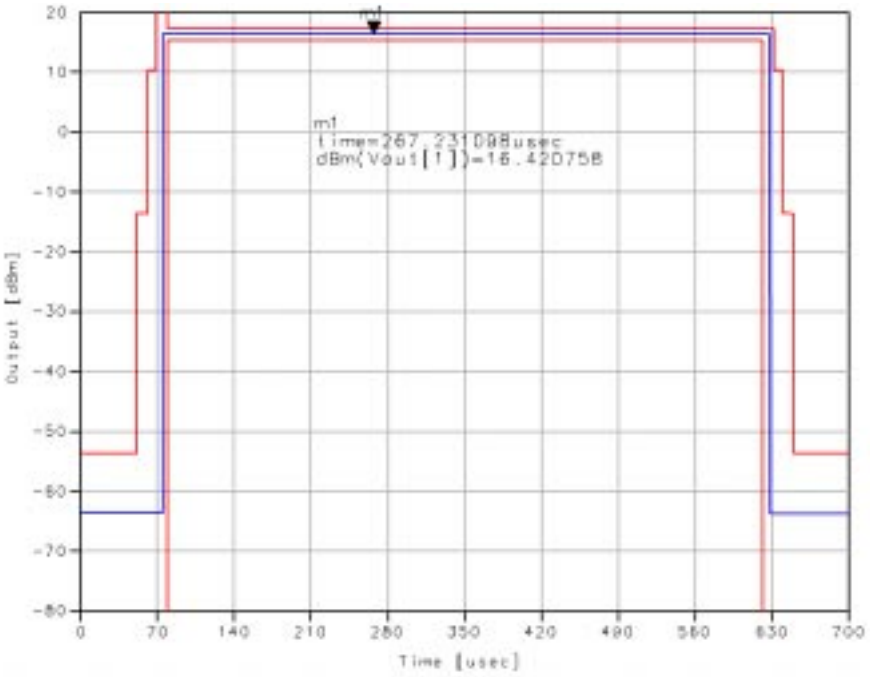


HEWLETT® PACKARD

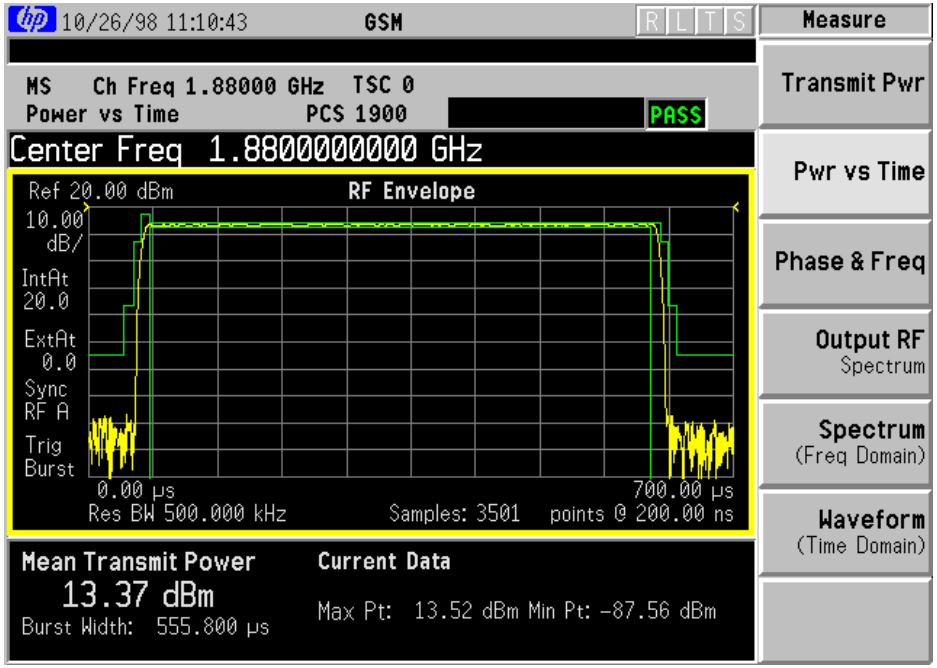
GSM Tests

Power versus Time

Simulation



Measured

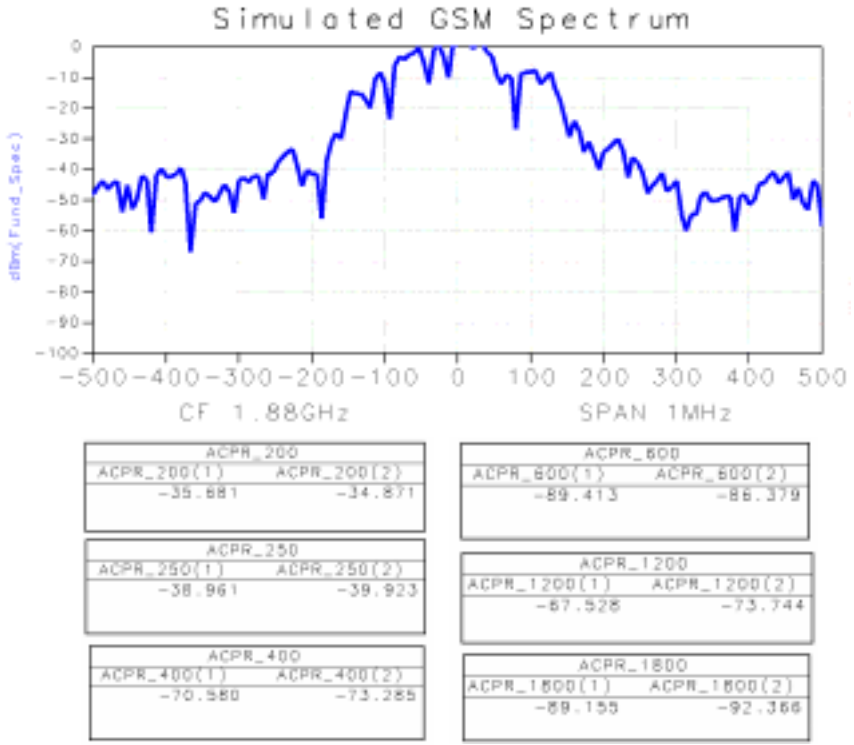


HEWLETT® PACKARD

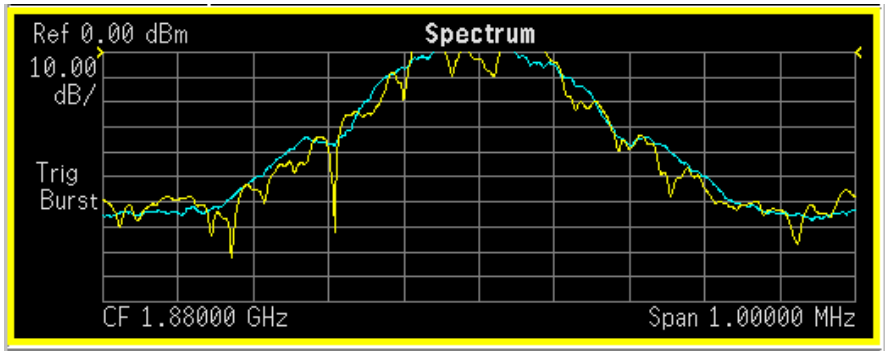
GSM Tests

Output RF Spectrum

Simulation



Measured



Modulation Ref Power: 5.6 dBm/ 30.000 kHz

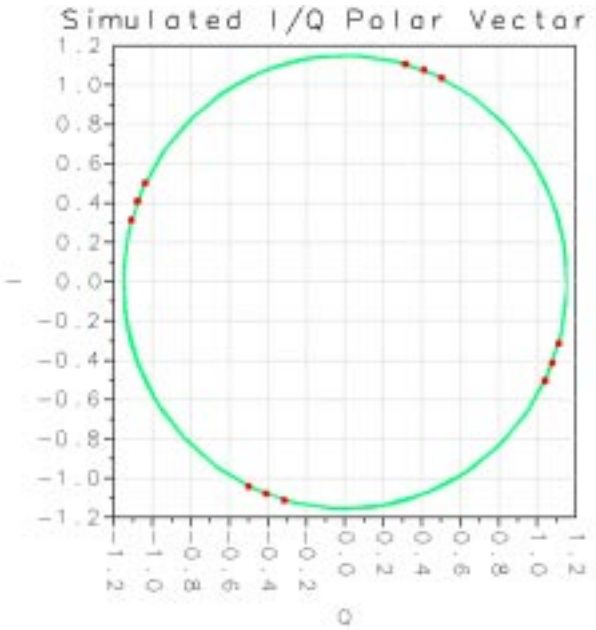
Offset Freq List: Short Sync RF A Trig Burst

		Lower		Upper	
Offset Freq	Res BW	dB	dBm	dB	dBm
200.000 kHz	30.000 kHz	-37.1	-31.5	-37.7	-32.1
250.000 kHz	30.000 kHz	-42.4	-36.8	-42.3	-36.7
400.000 kHz	30.000 kHz	-69.1	-63.5	-66.2	-60.7
600.000 kHz	30.000 kHz	-81.2	-75.6	-78.6	-73.0
1.20000 MHz	30.000 kHz	-84.7	-79.1	-81.3	-75.7
1.80000 MHz	100.000 kHz	-73.1	-67.5	-76.2	-70.6

GSM Tests

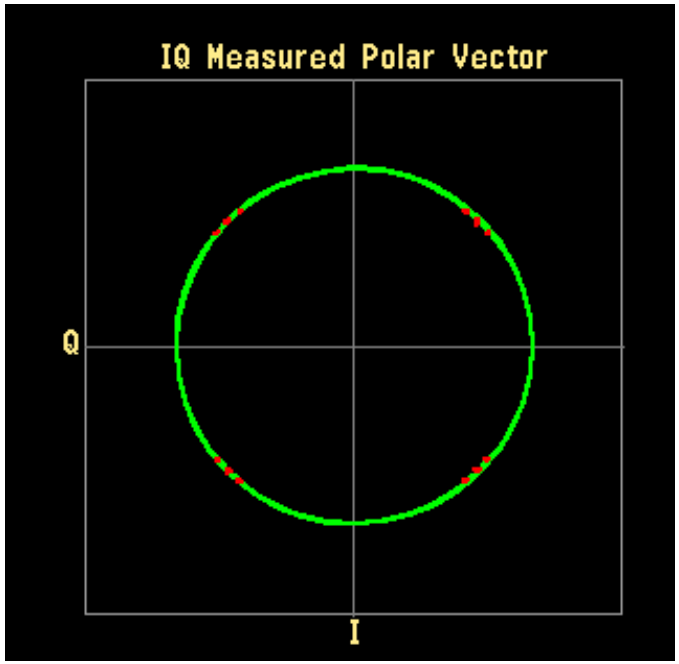
Phase and Frequency Error

Simulation



Phase Error < 1deg
Freq. Error < 5 Hz

Measured

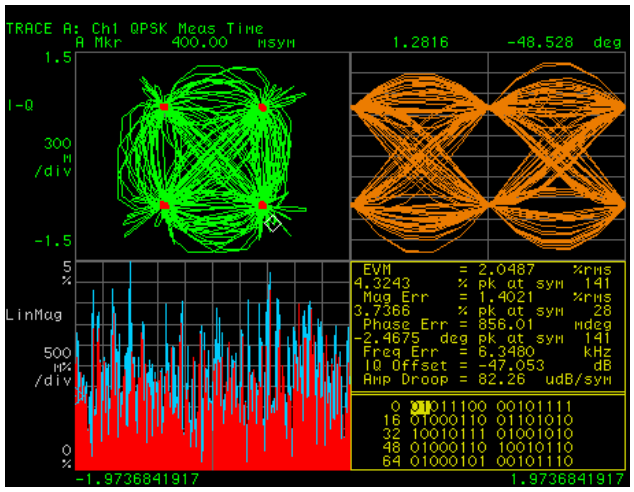


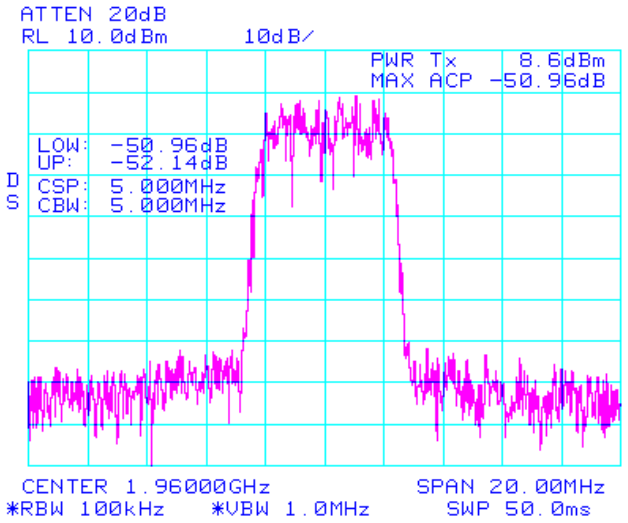
Phase Error < 1deg
Freq. Error < 5 Hz

HEWLETT® PACKARD

1G → 2G → 3G

- *Wider Bandwidths*
- *More Capacity*
- *Higher Data Rates*
- *W-CDMA Proposed*





HEWLETT® PACKARD

HP W-CDMA Solutions

HP ESG D-series RF Signal Generator with Option H97 Multi-code channel W-CDMA Personality, Option UND Dual Arbitrary Waveform Generator, Option H98 W-CDMA Real-time coding and Option H99 enhanced ACPR.

HP 8563E Option K35
Spectrum Analyzer and
W-CDMA ACPR Test Set

HP 89400 Series
W-CDMA Measurement System

HP E8851A Communications Systems Designer +
W-CDMA Design Library

HP 71910P Wideband Receiver
HP 89410A Vector Signal Analyzer for
20 MHz demodulation bandwidth

HEWLETT® PACKARD

References and More Information

- ***CDMA - www.cdg.org***

- ***GSM - www.gsmdata.com***

- ***W-CDMA - www.hp.com***