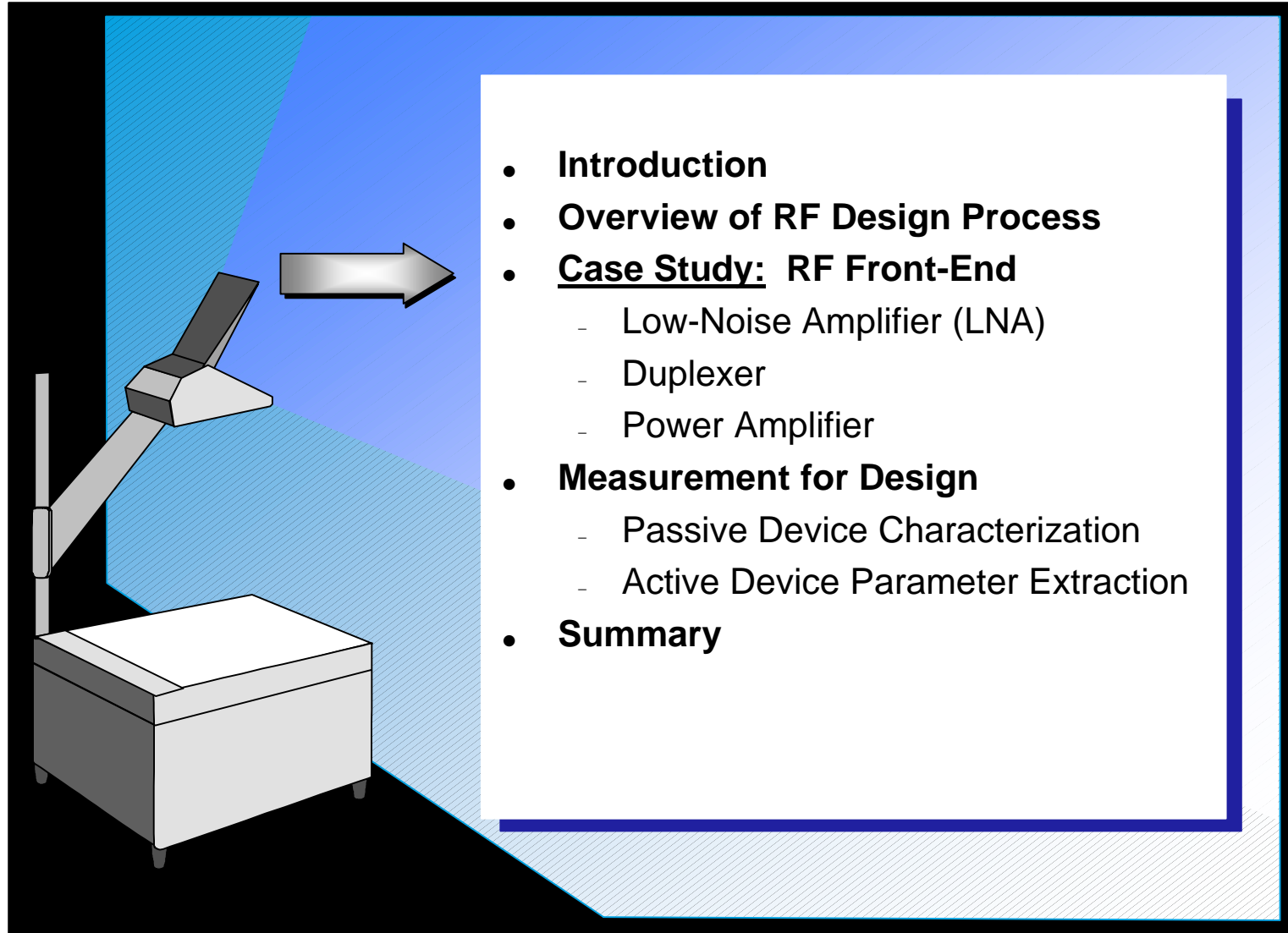
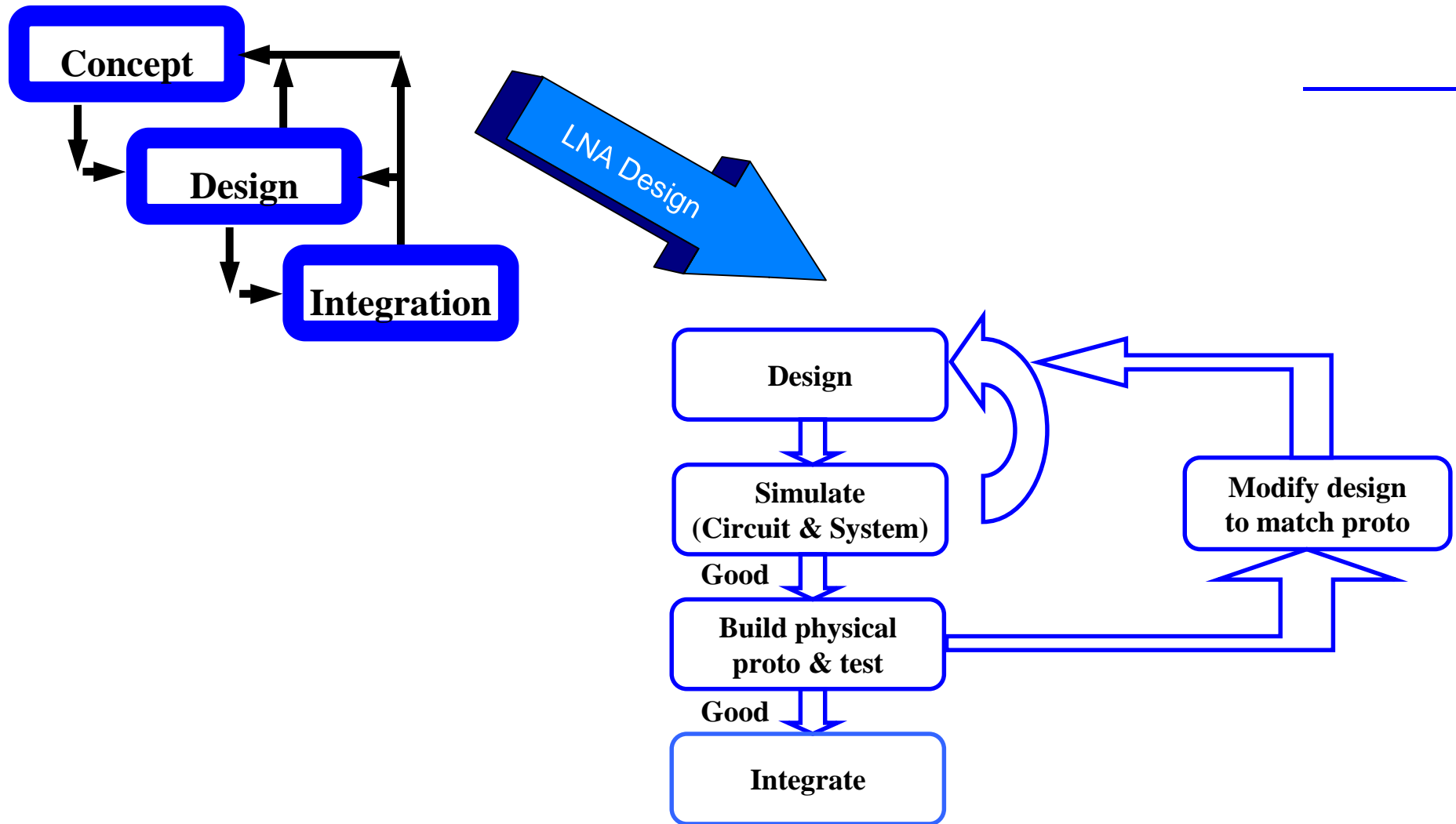


Agenda



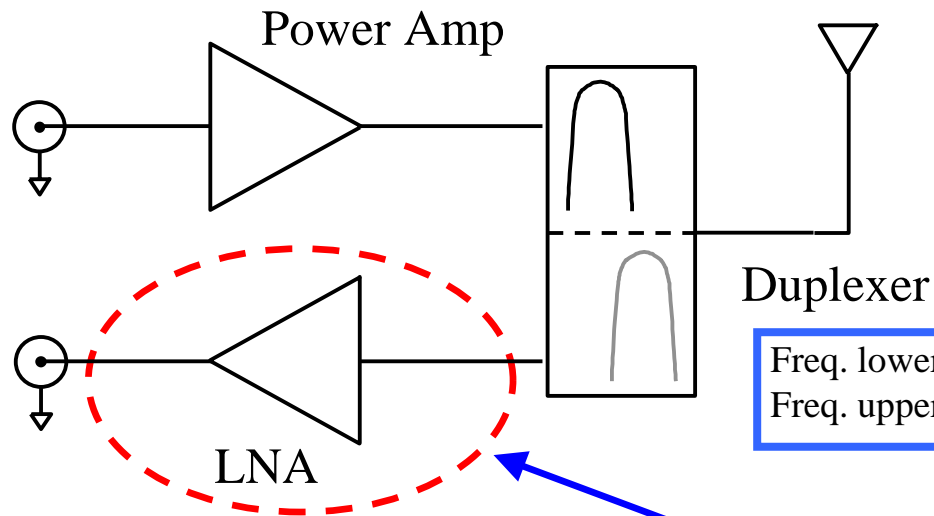
- Introduction
- Overview of RF Design Process
- **Case Study: RF Front-End**
 - Low-Noise Amplifier (LNA)
 - Duplexer
 - Power Amplifier
- **Measurement for Design**
 - Passive Device Characterization
 - Active Device Parameter Extraction
- **Summary**

Design Cycle Case Study: LNA



Concept: System-Level Design (Simple PCS-band transceiver front end)

Freq. = 1880 MHz +/- 50 MHz min.
Pout (1 dB) = +25 dBm min
Psat = +27 dBm min
Gain = + 24 dB min



Freq. lower band = 1880 MHz +/- 30 MHz
Freq. upper band = 1960 MHz +/- 30 MHz

Freq. = 1960 MHz +/- 50 MHz min
Gain = + 25 dB min
NF < 2.5 dB

**The first part of the case study
will focus on the LNA**

What Are My Resources?



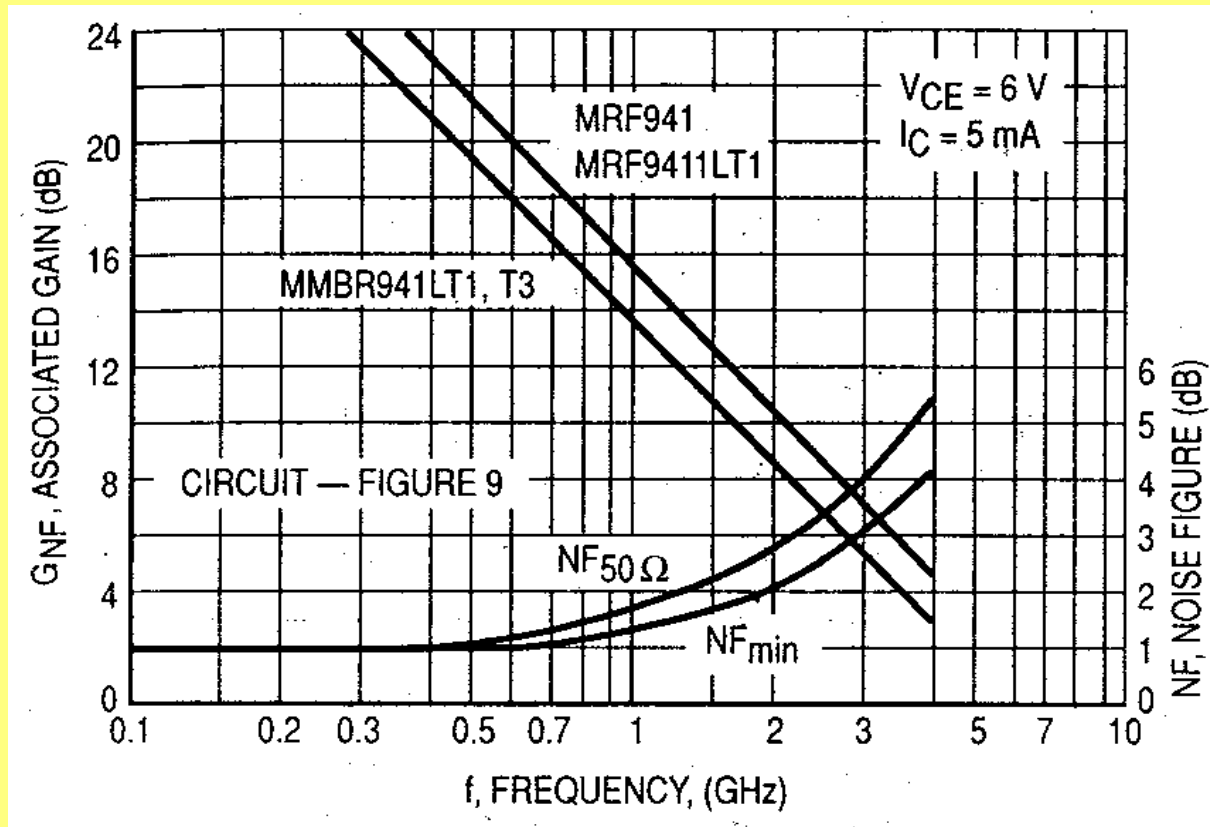
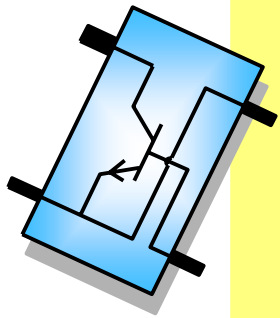
How do I design a low-noise amplifier?

- Talk with experienced people
- Textbooks
- Magazines (e.g., *RF Design*)
- Classes
- Purchase from third-party

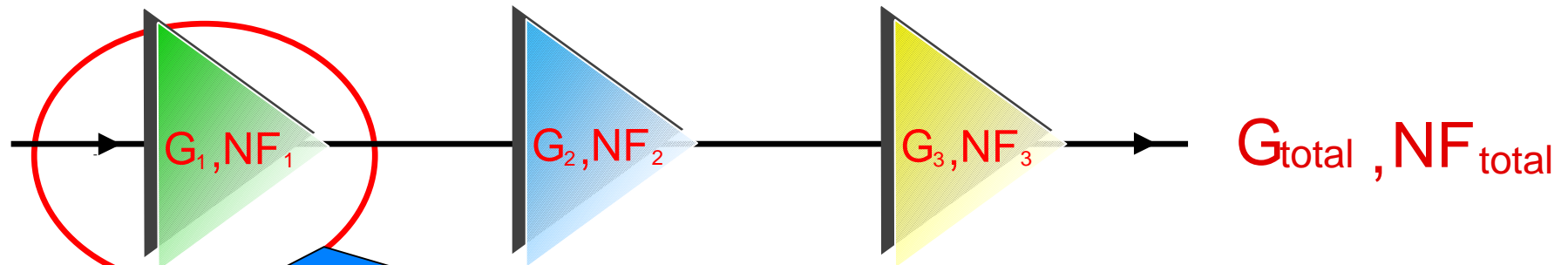


Choosing a Device

A typical low-noise device

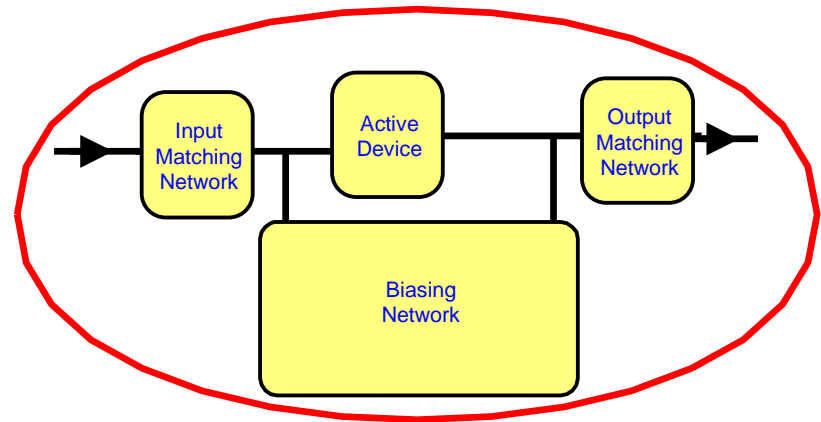


Amplifier Stage Design

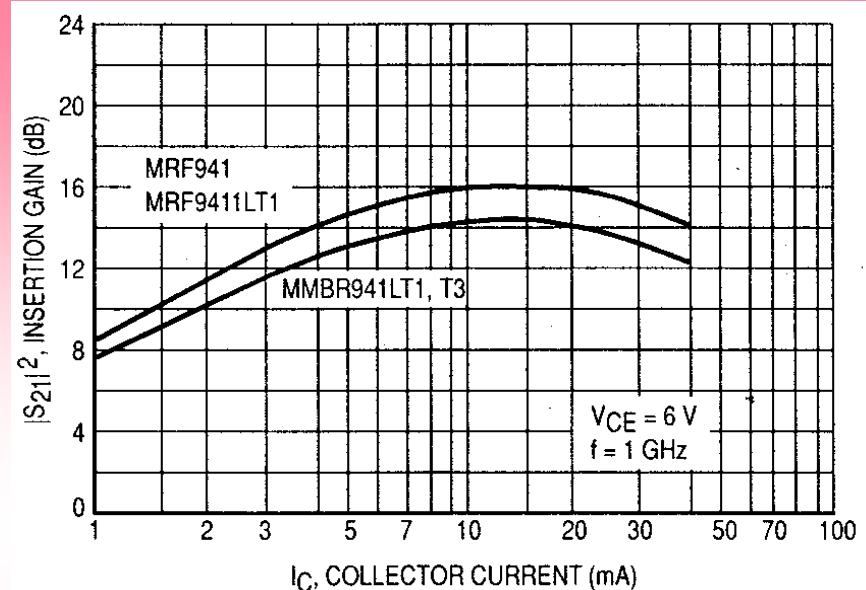
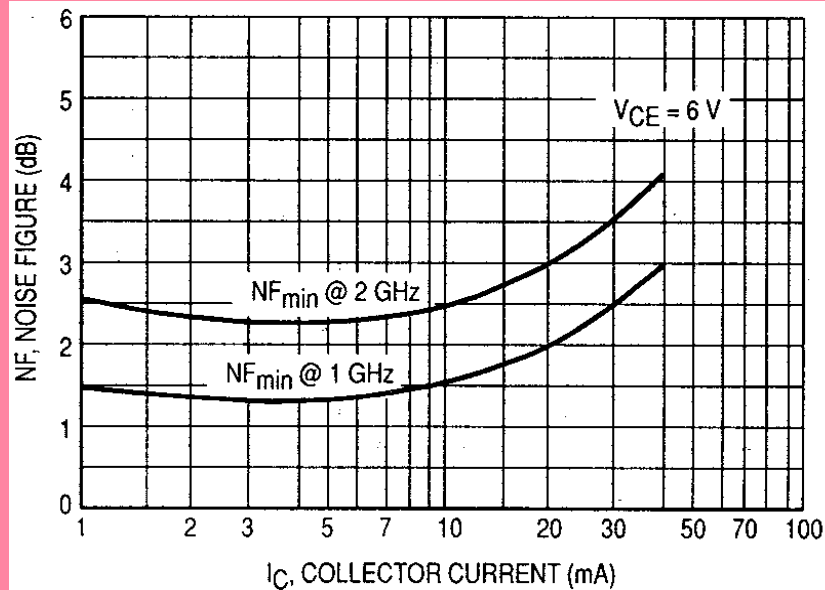


$$G_{total} = G_1 G_2 G_3 \dots$$

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + \frac{NF_3 - 1}{G_1 G_2} + \dots$$



Transistor Biasing



- Decide on bias currents and voltages
- Find values for biasing resistors
- Verify values using DC analysis with the nonlinear model
- Design from available power supplies
- Check power dissipation

Input Matching Network

Gain Circles:

Max. Gain: 8.6
dB

-1.0 dB

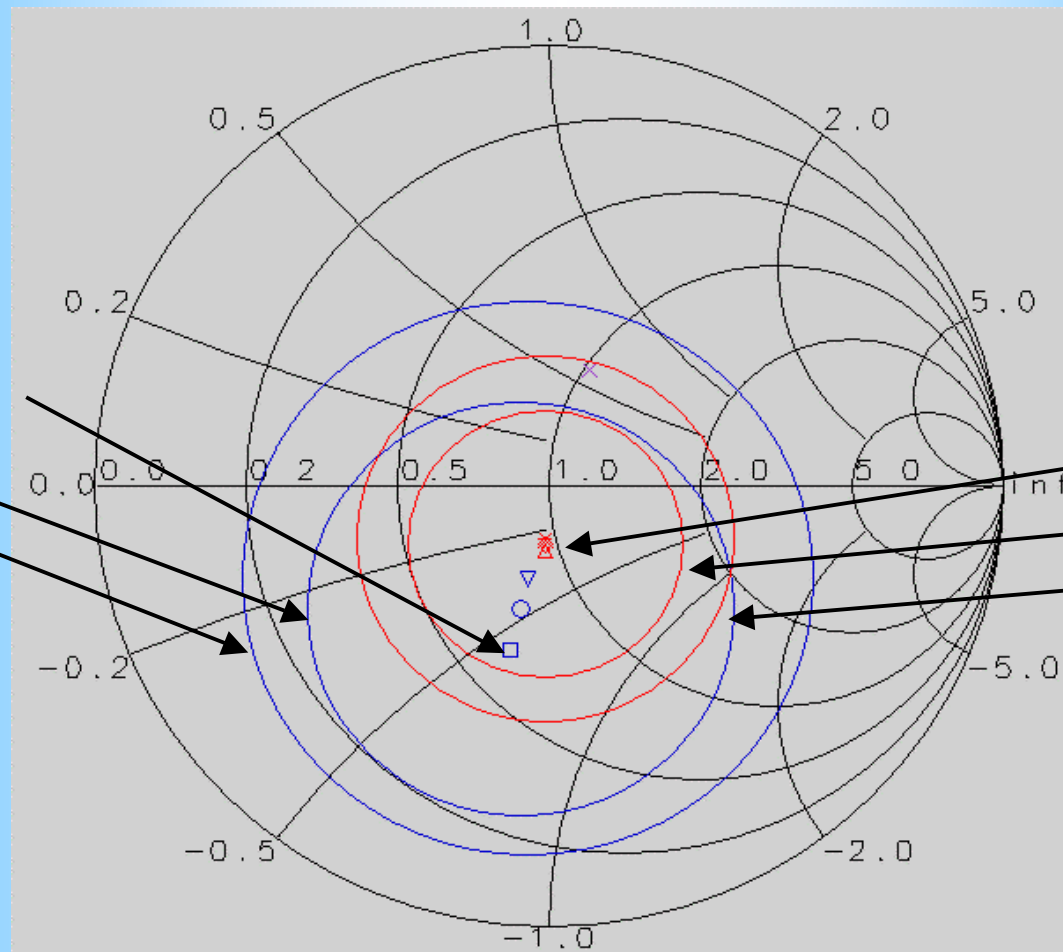
-2.0 dB

Noise Circles:

Min. Noise: 1.8 dB

+0.25 dB

+0.50 dB

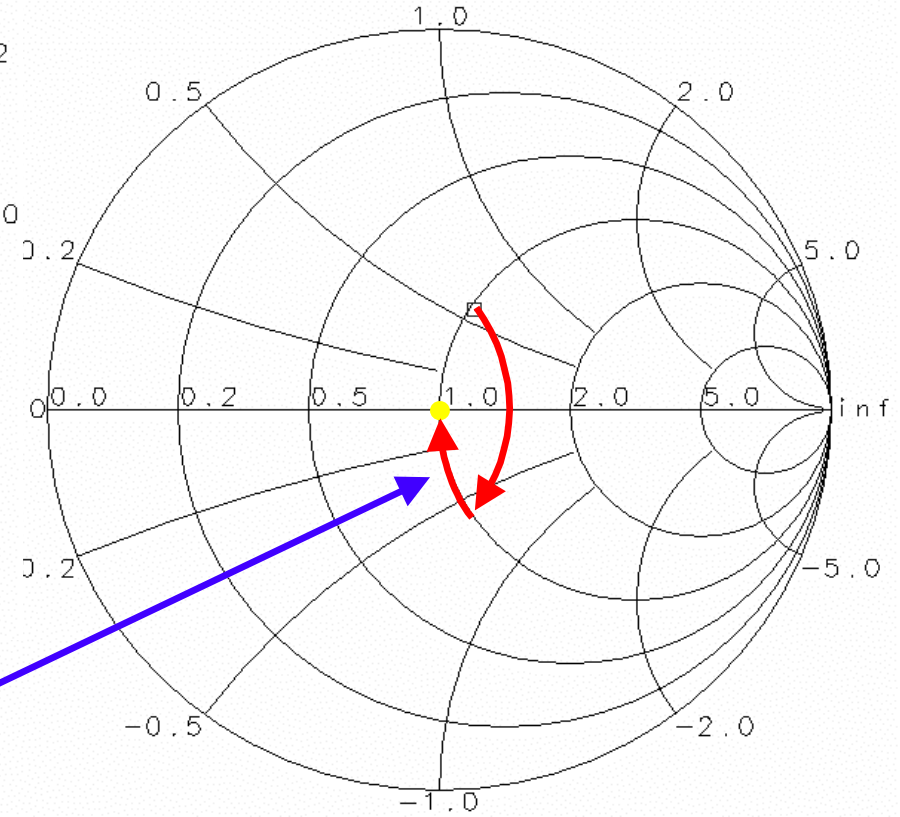
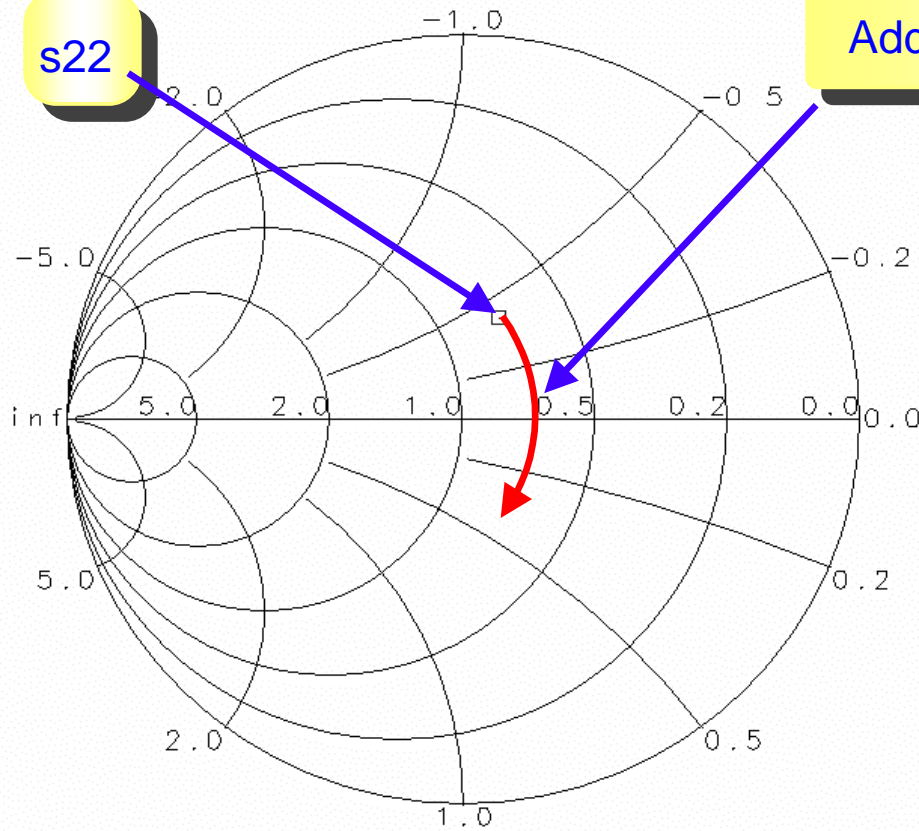


Notice that the match for maximum gain is not the same as the match for minimum noise figure

Output Matching Network

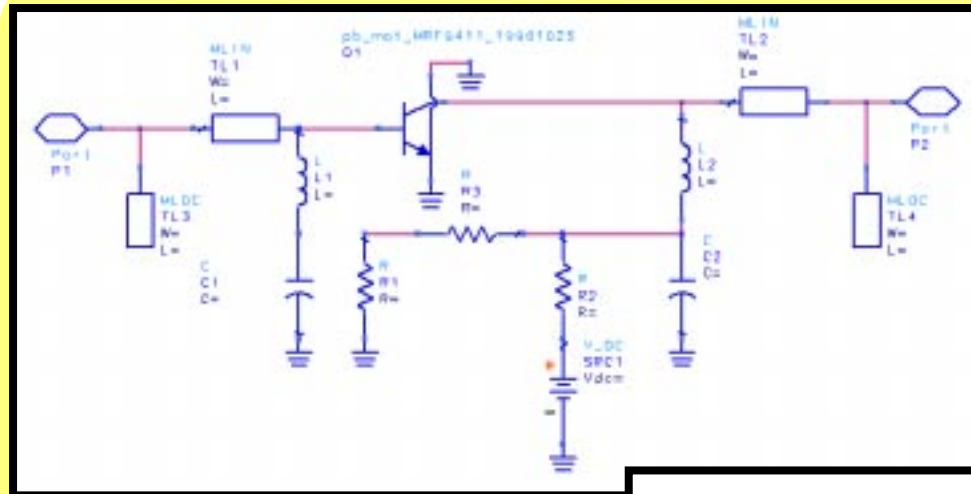
s22

Add shunt capacitance on admittance chart

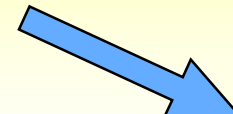


Add series inductance on impedance chart

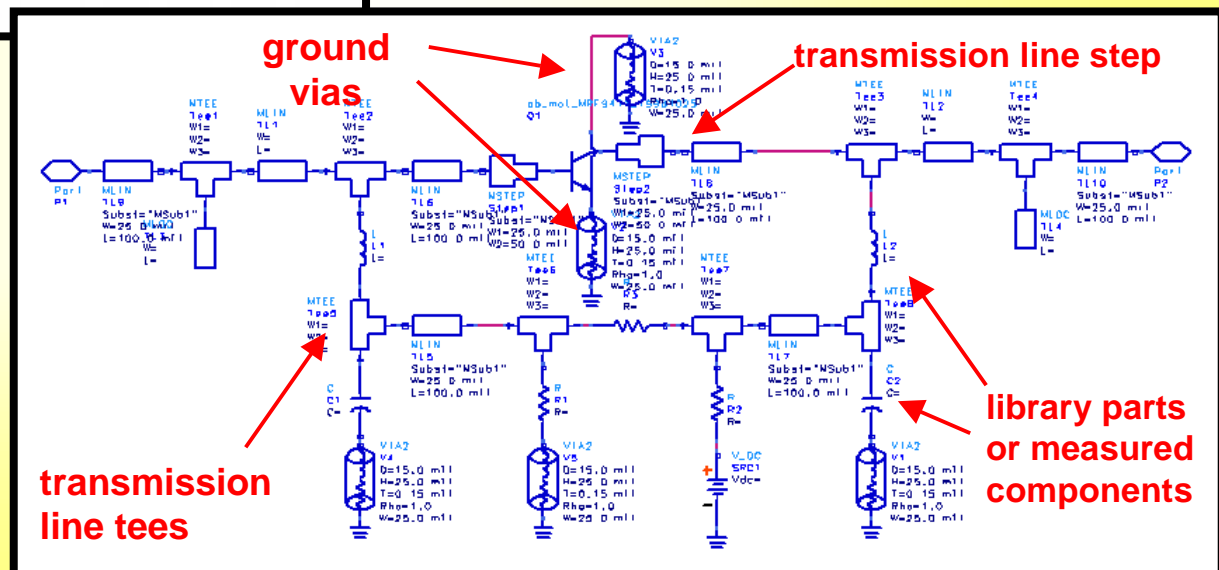
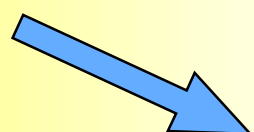
Refining your Design



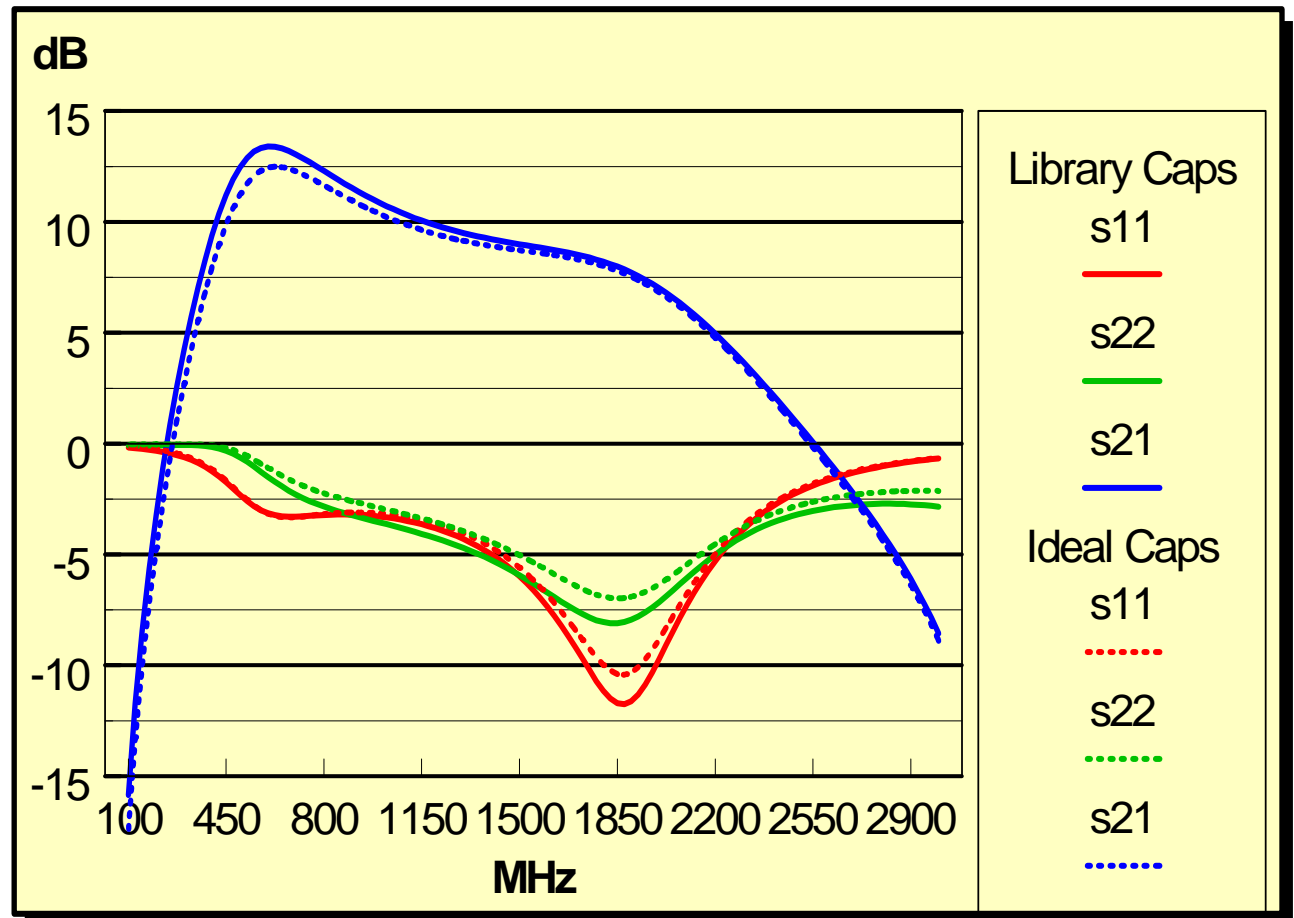
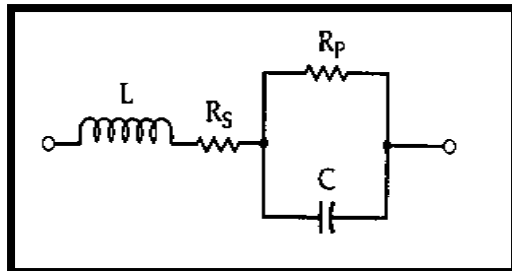
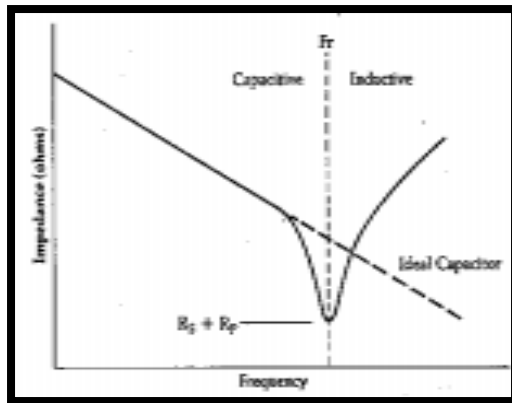
from ideal...



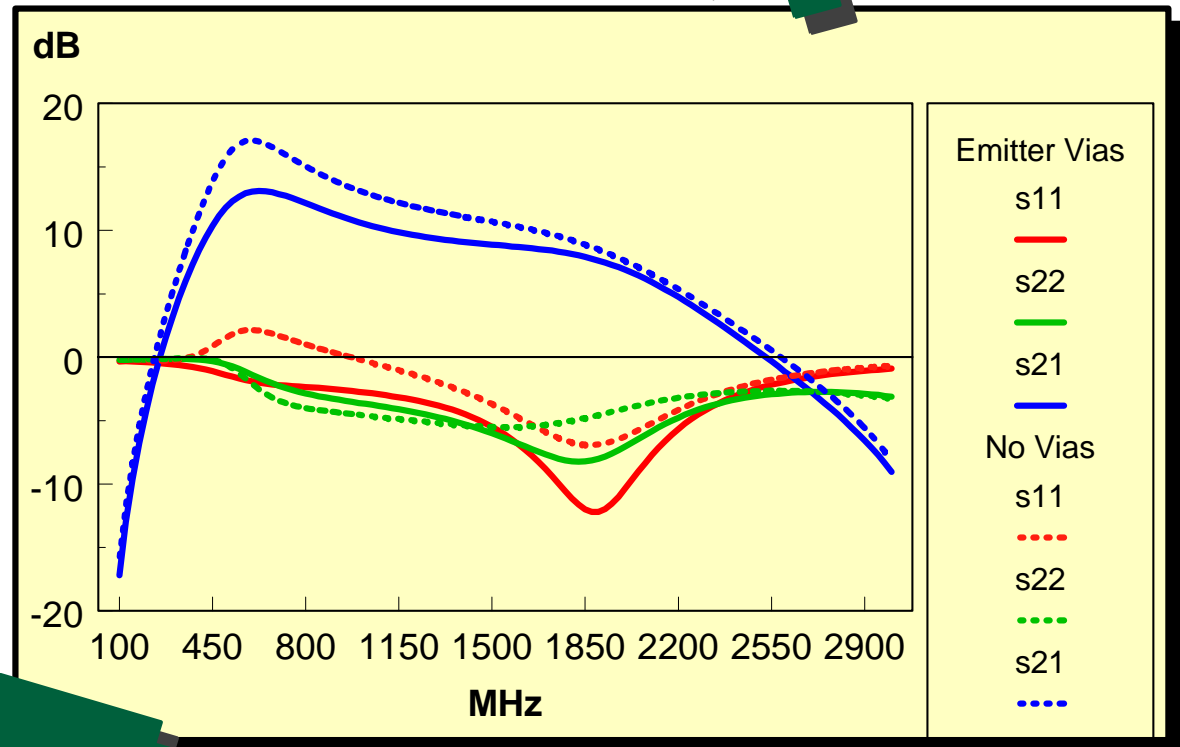
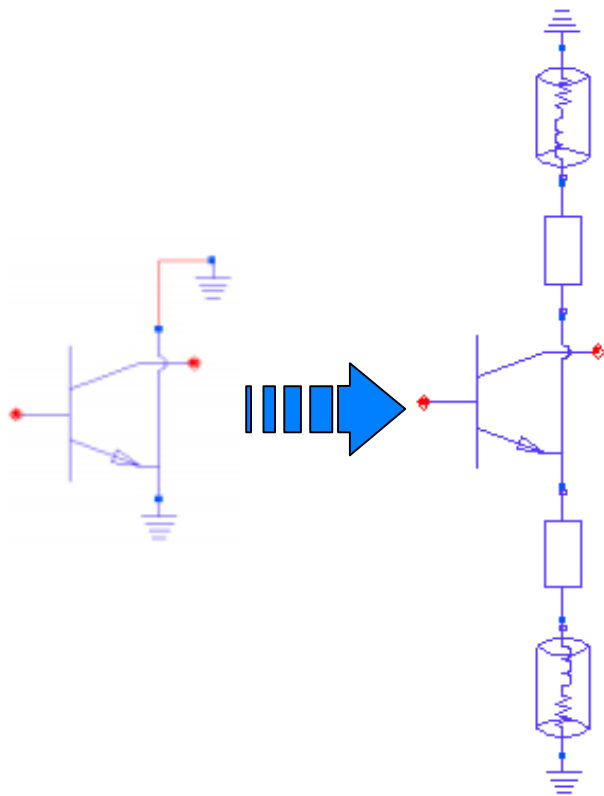
...closer to reality



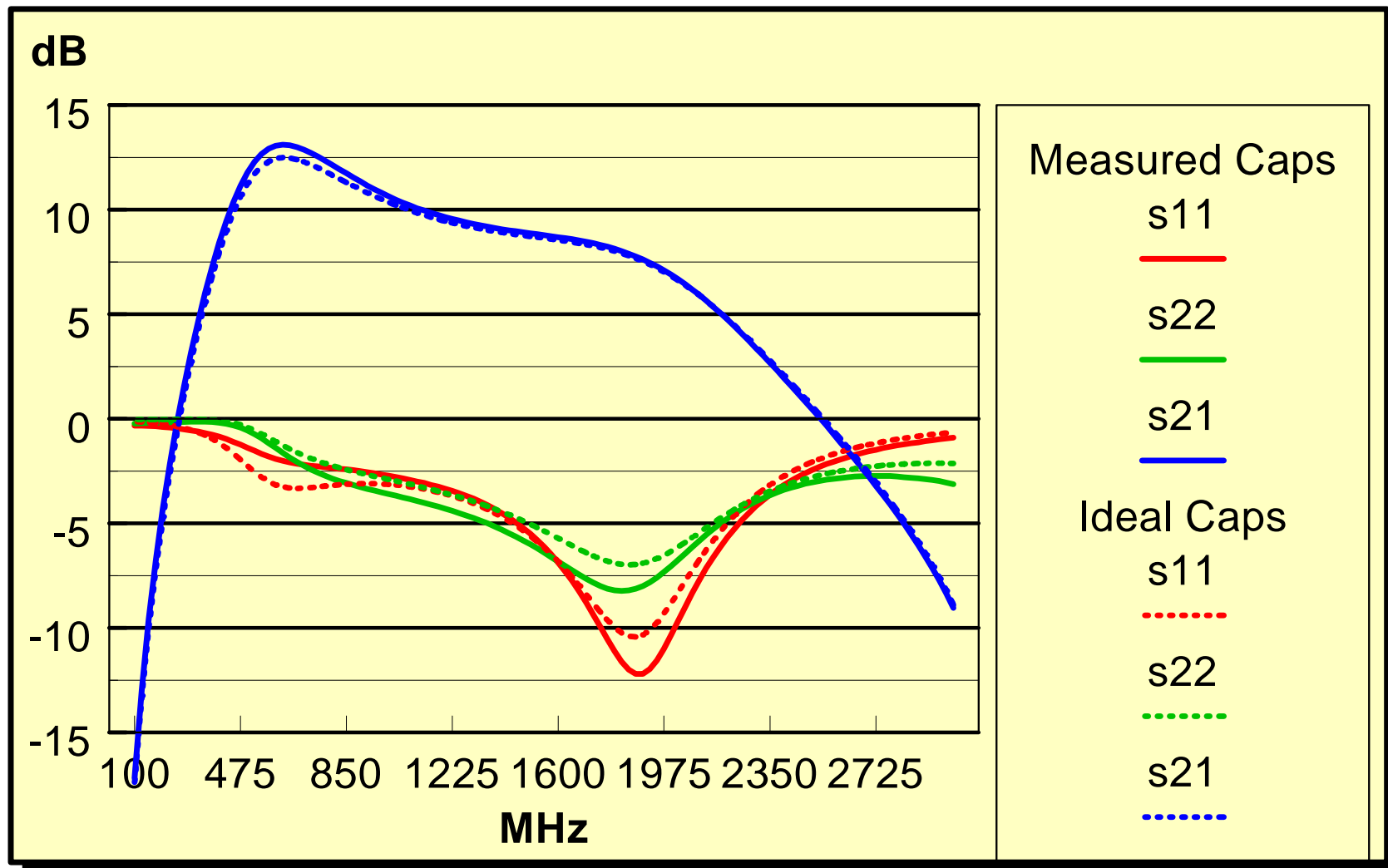
Refine Design with Library Parts



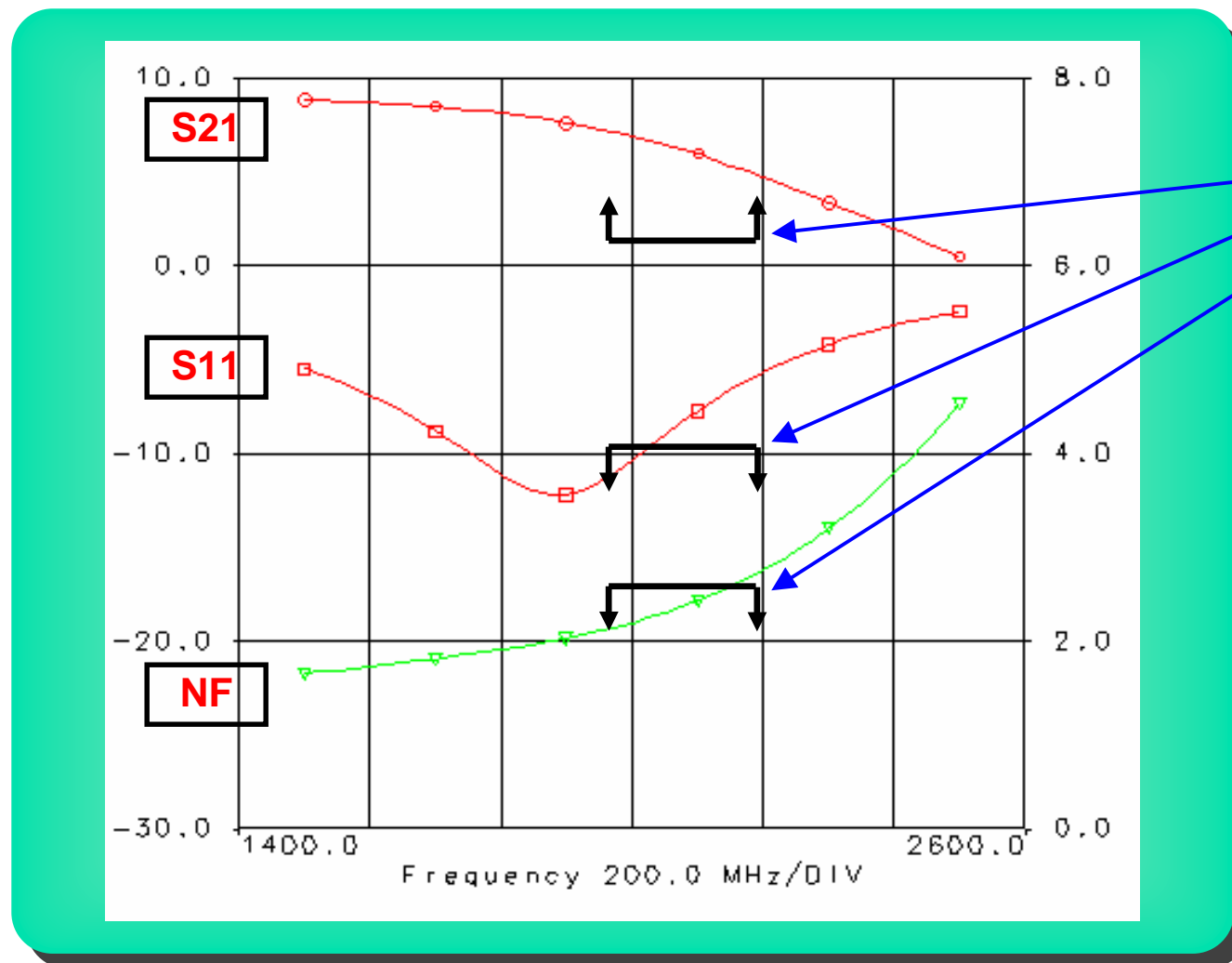
Adding Interconnection Refinements



Measured vs. Ideal Capacitors



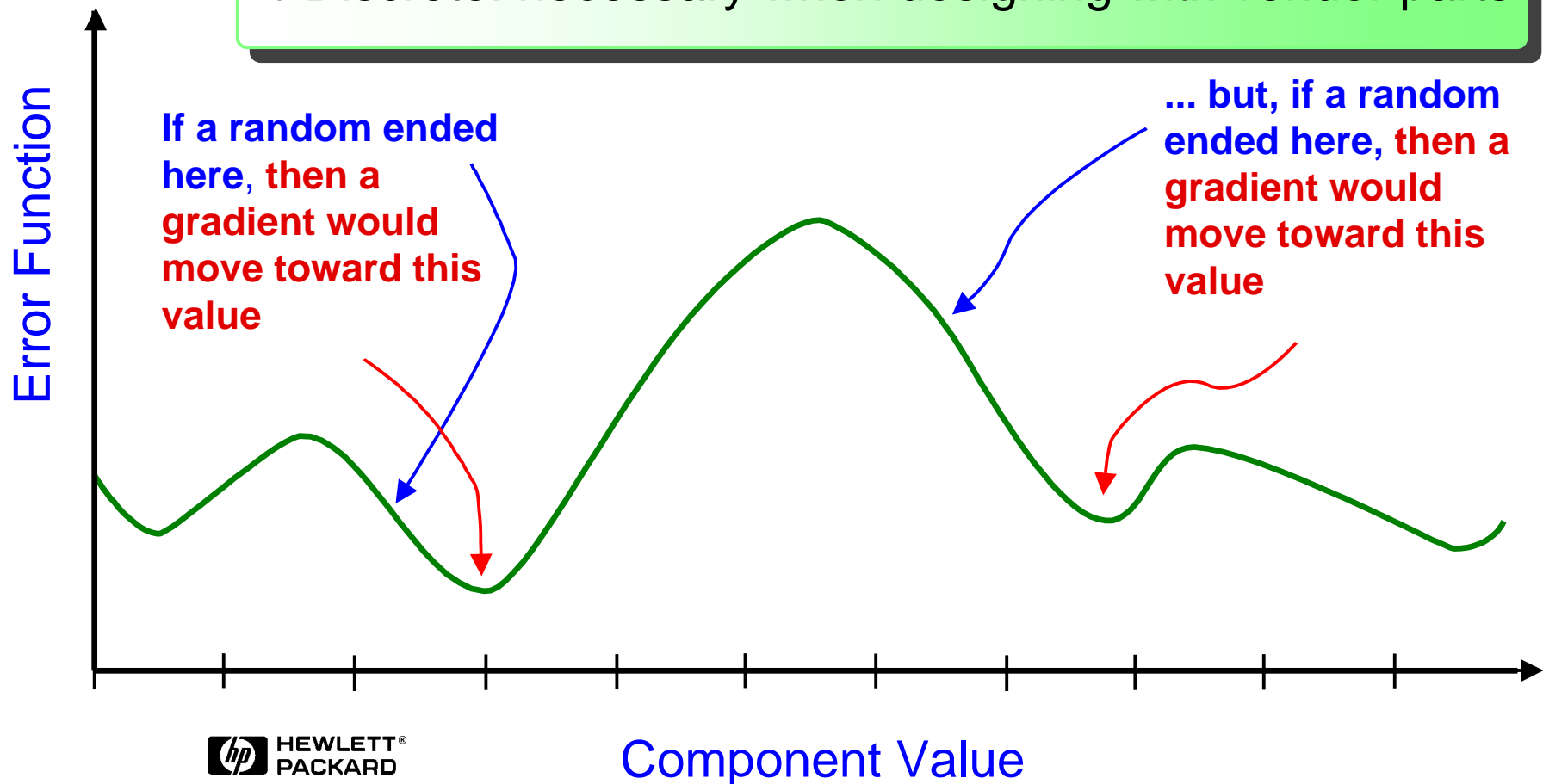
Performance Optimization



Goals

Search Methods

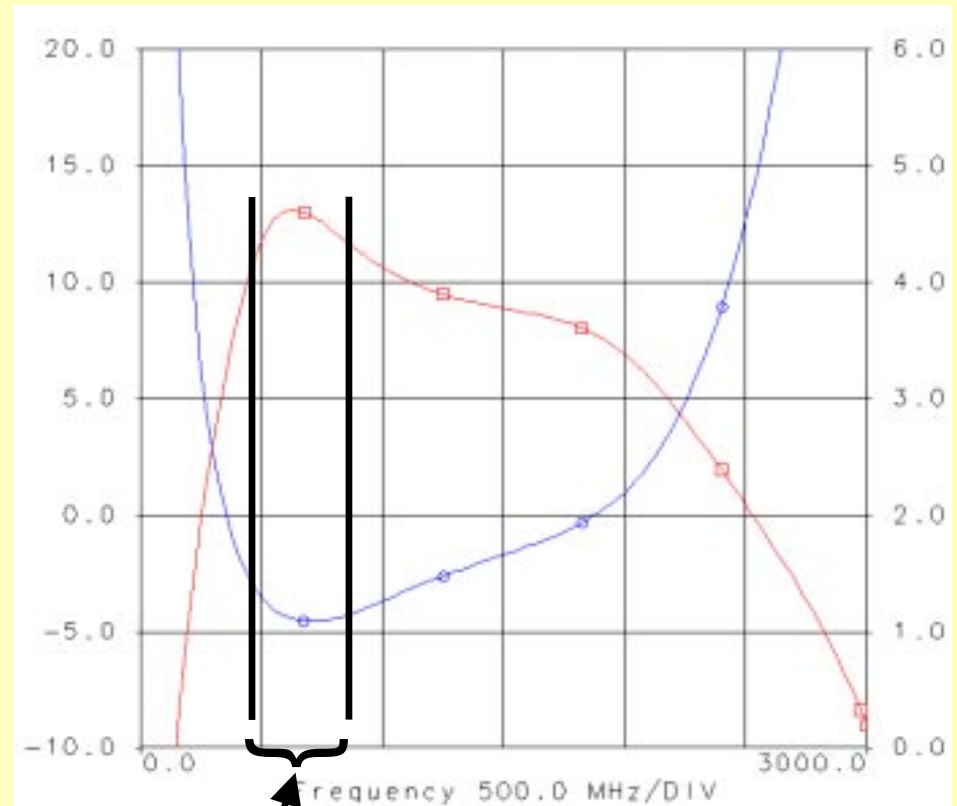
- Random: approaches global minimum error function
- Gradient: zeros-in on local minimum error function
- Discrete: necessary when designing with vendor parts



Problems with the Breadboard

Things to look for when troubleshooting:

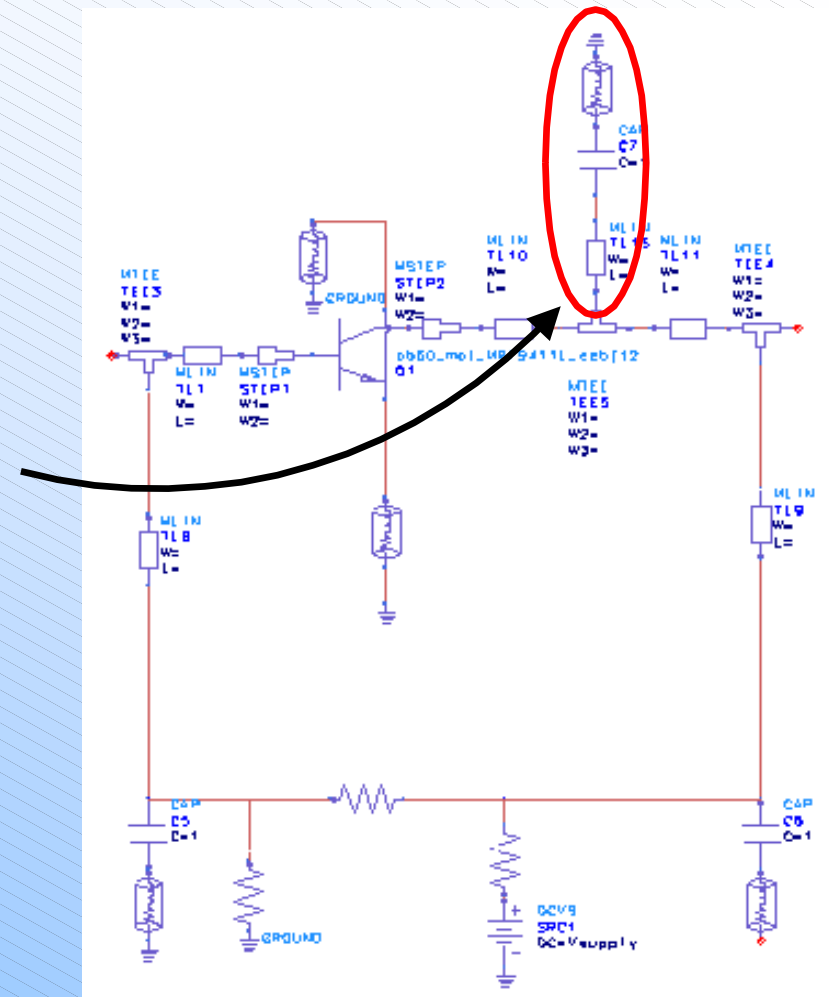
- Stability at all frequencies
- Biasing problems
- System interactions



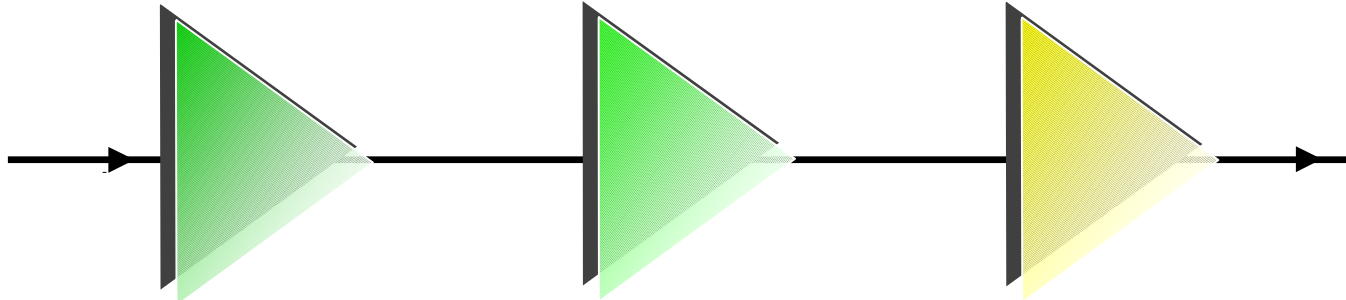
Removing the Oscillation

Hypothesis: collector impedance is too high at lower frequencies

- Remove oscillation by lowering collector impedance at problem frequencies (while maintaining correct impedance in the desired band)
- Shorted stub on the collector



Combined Breadboard

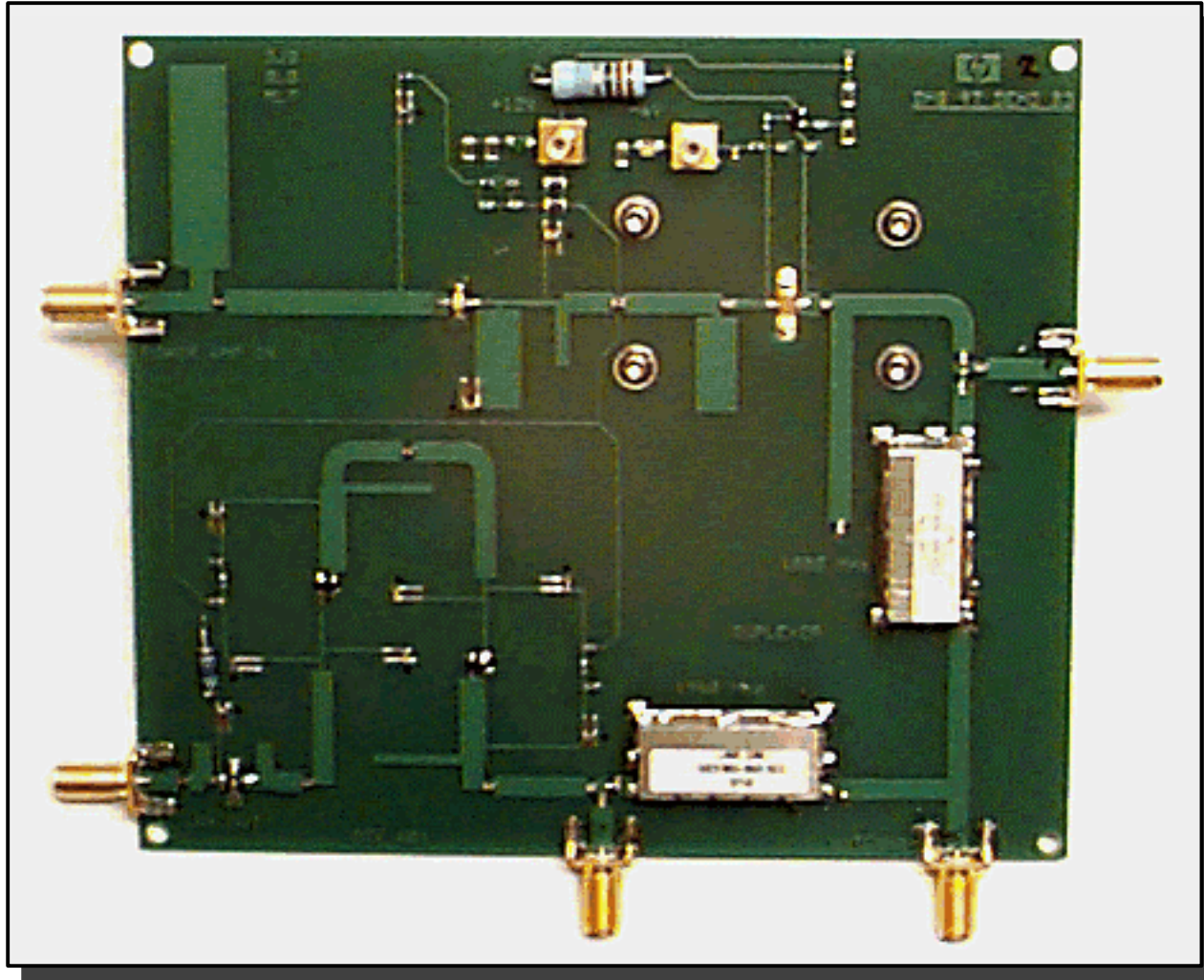


- Three stages
 - Stages 1 & 2: low-noise (identical stages)
 - Stage 3: supply the rest of the desired gain

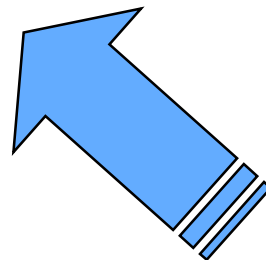
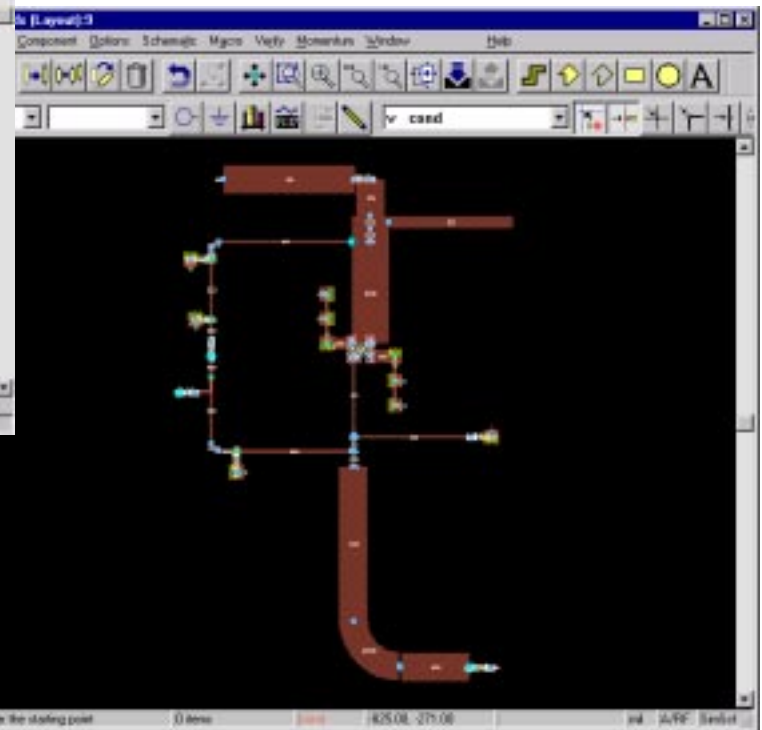
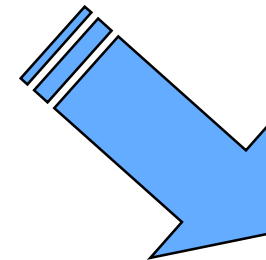
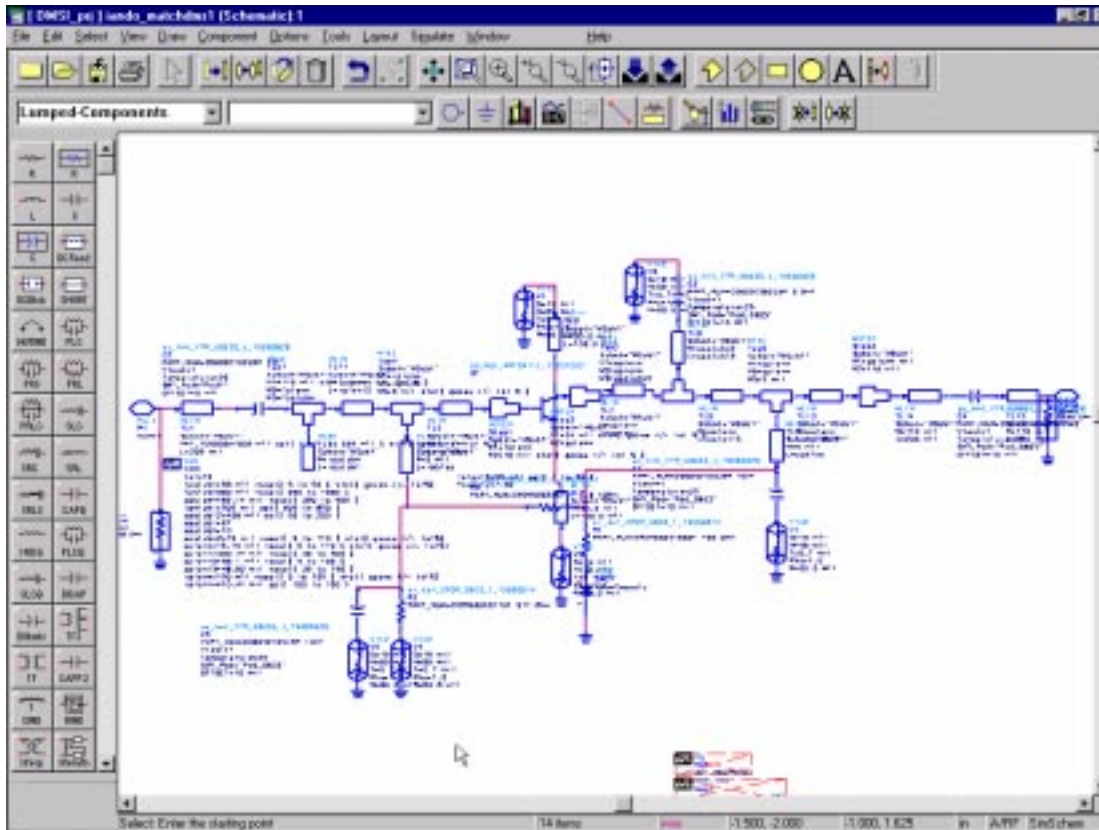
Combining Issues

- Stability: if even one stage is conditionally stable, circuit may oscillate
- Matching: small mismatches individually, can become worse collectively

Build the Prototype

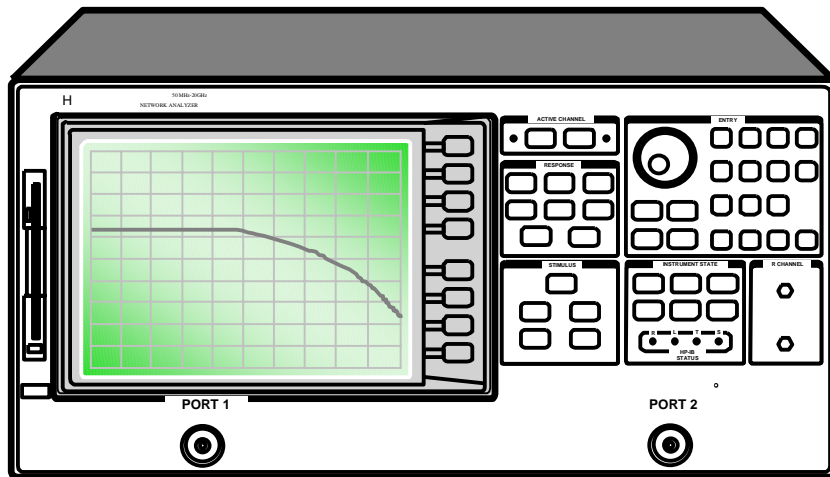


Layout & Design Synchronization

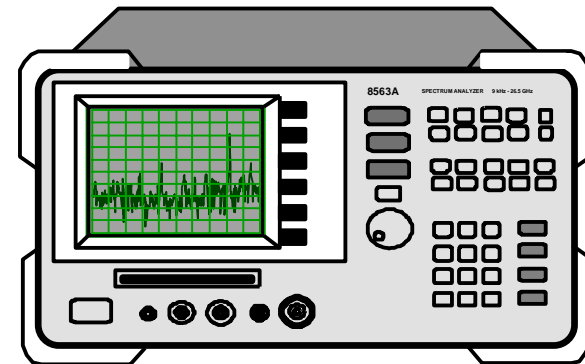


Design Verification

- Bias up circuit - check voltages
- Physical check to see if any resistor, device, etc. is warm
- Check for oscillations
- If all looks good -- measure

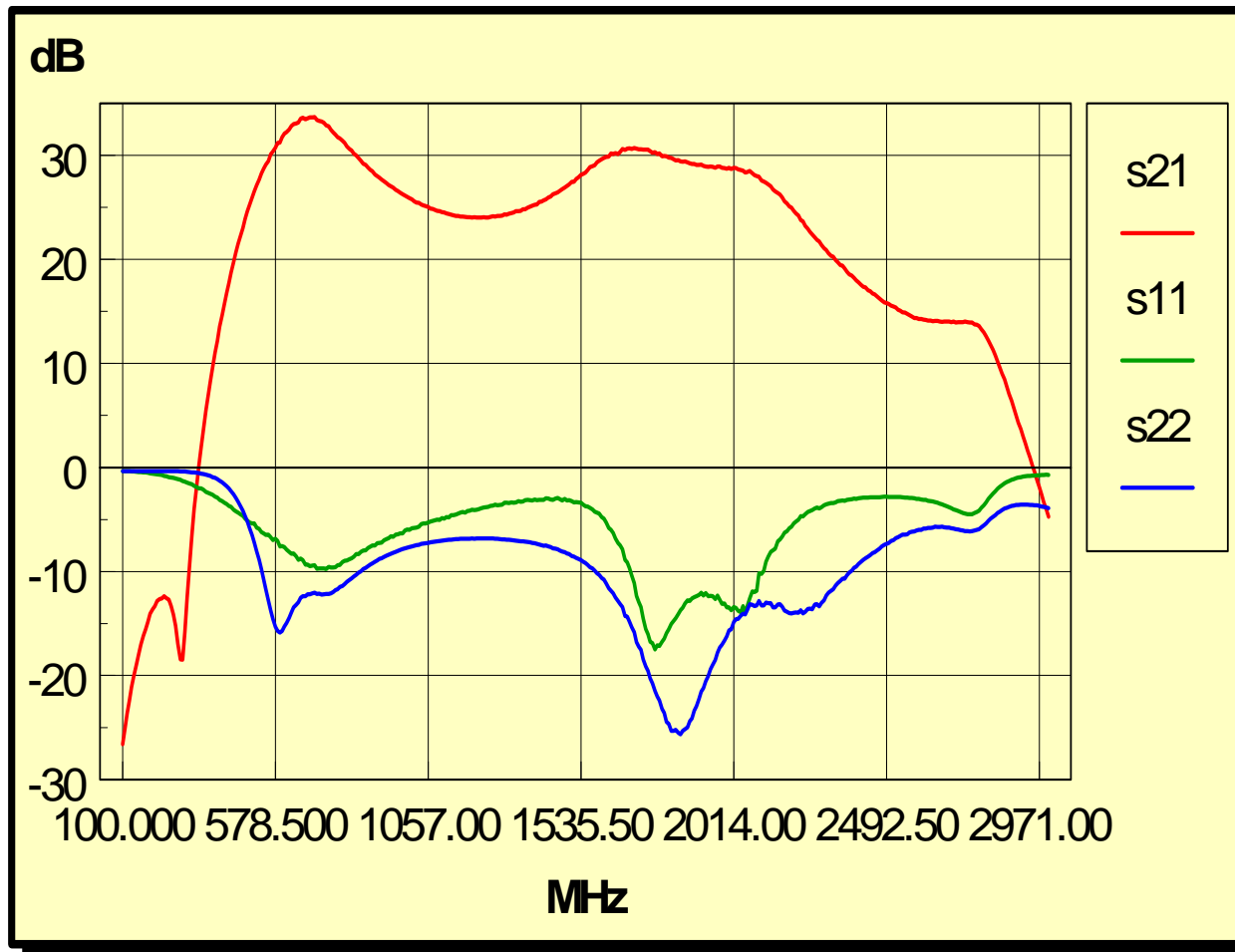


.gain
.input/output matches

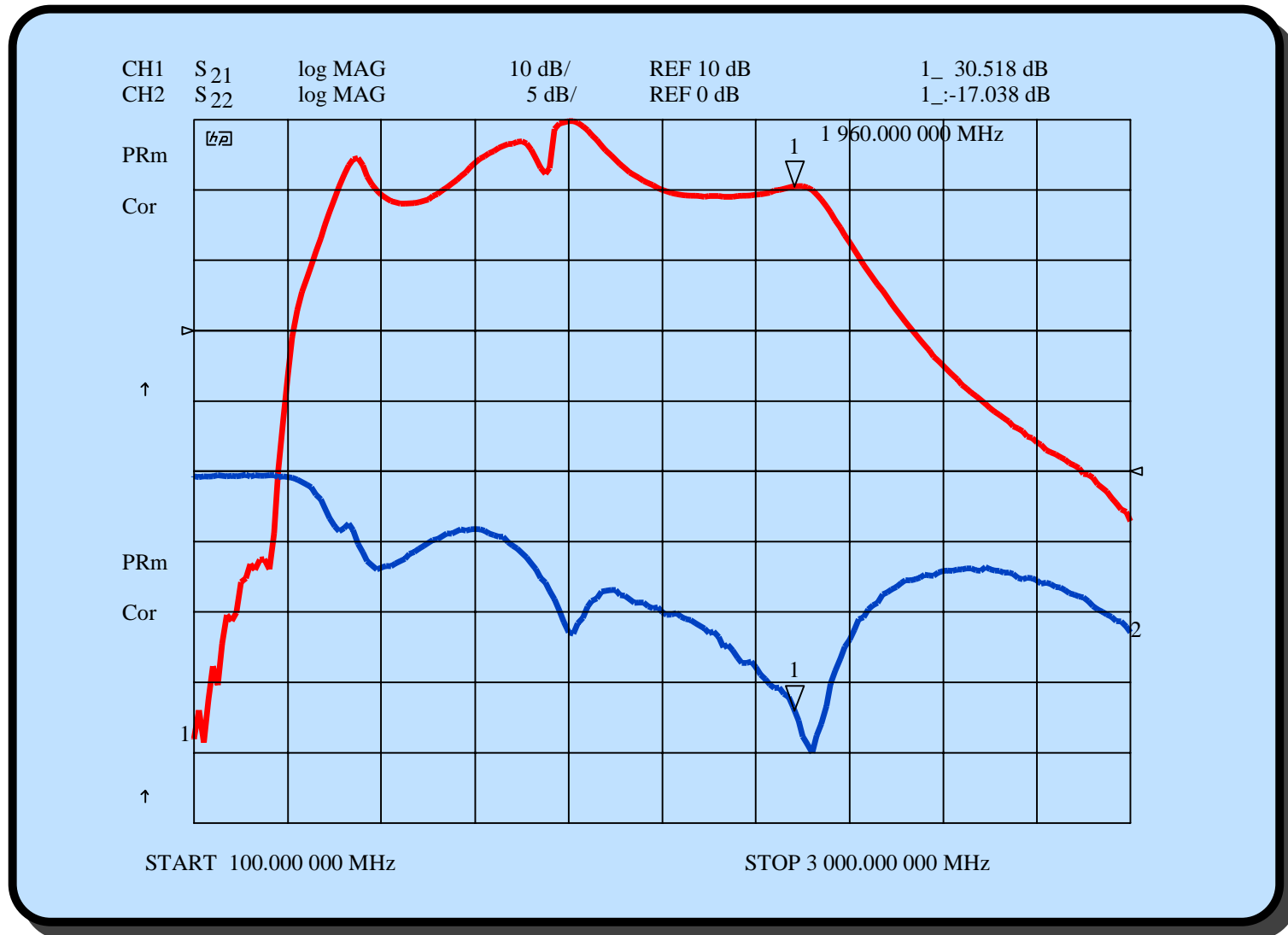


.noise figure
.oscillations

Simulated Gain and Match

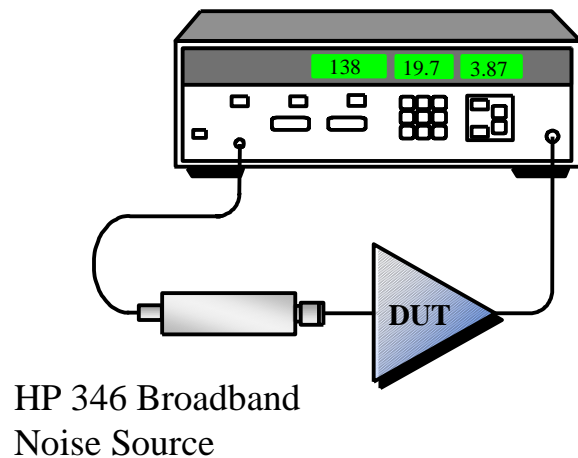


Measured Gain and Output Match



Measuring Noise Figure

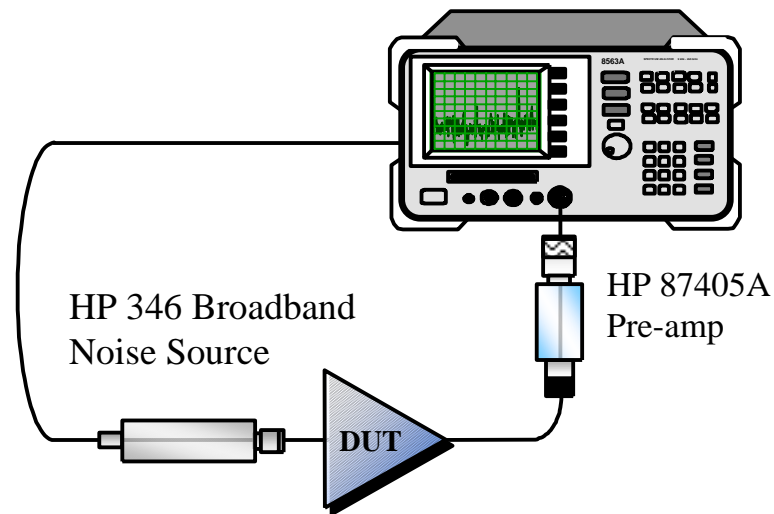
HP 8970B Noise Figure Meter



- High accuracy (± 0.1 dB)

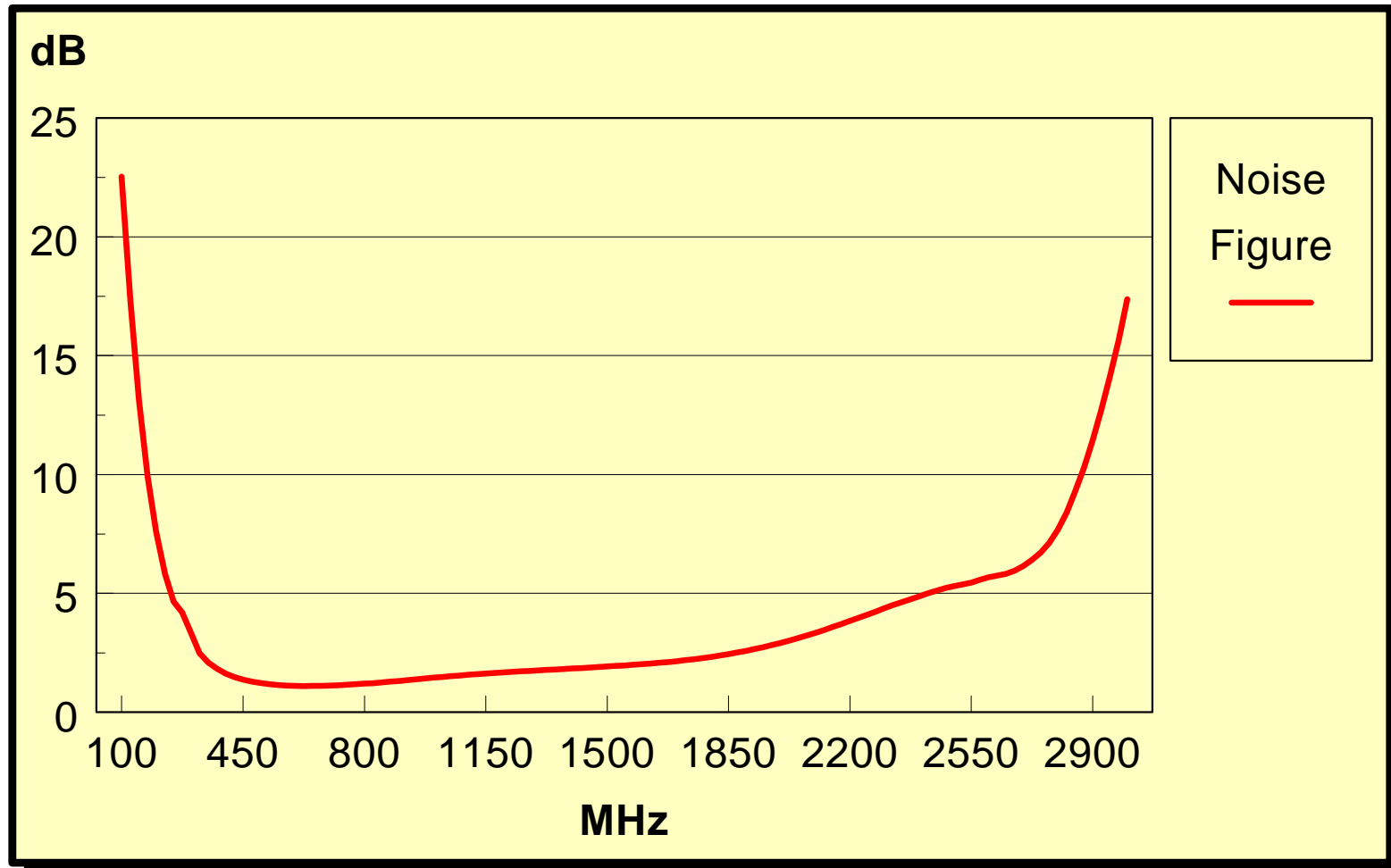
Both solutions measure:
Noise figure and gain
CW or swept frequency

HP 8590 E-Series Spectrum Analyzer w/
HP 85719A Noise Figure Personality

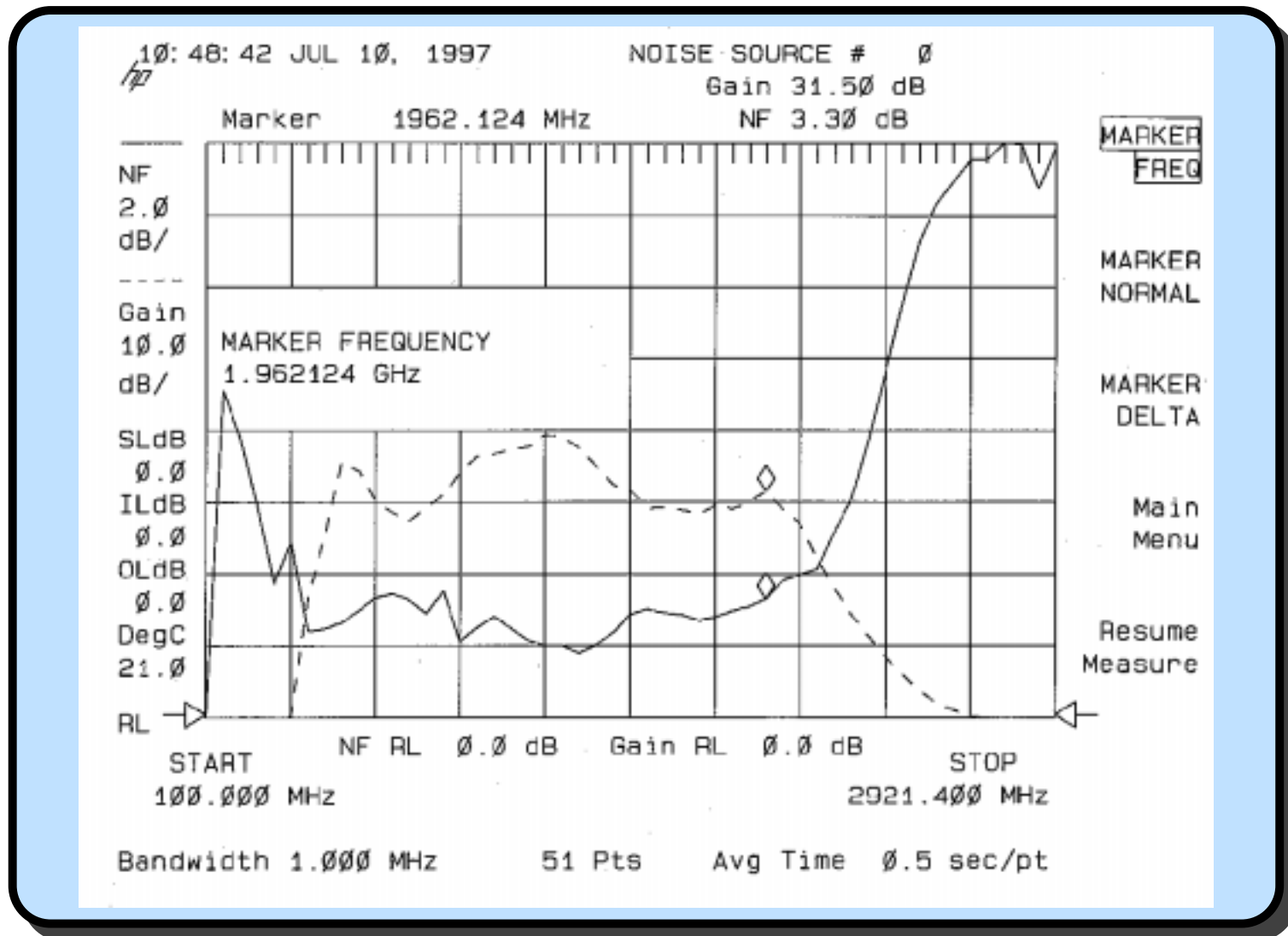


- Medium accuracy (± 0.5 dB)
- Variable IF bandwidths
- Averaging
- Measurement versatility

Simulated Noise Figure

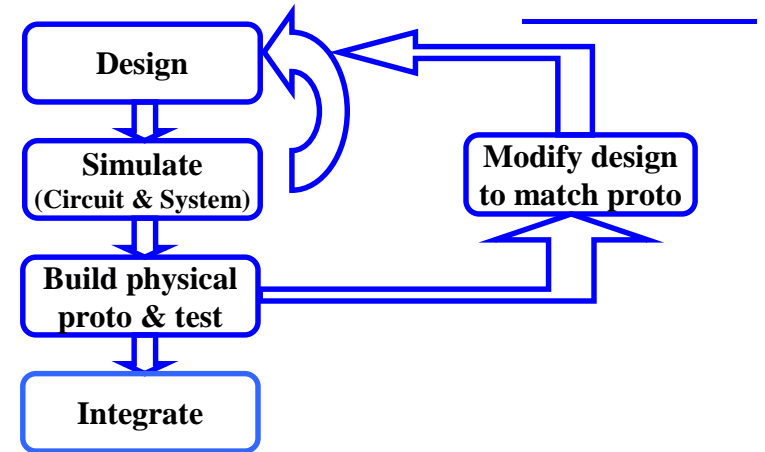


Measured Noise Figure



Modify Circuit Design to Match Proto

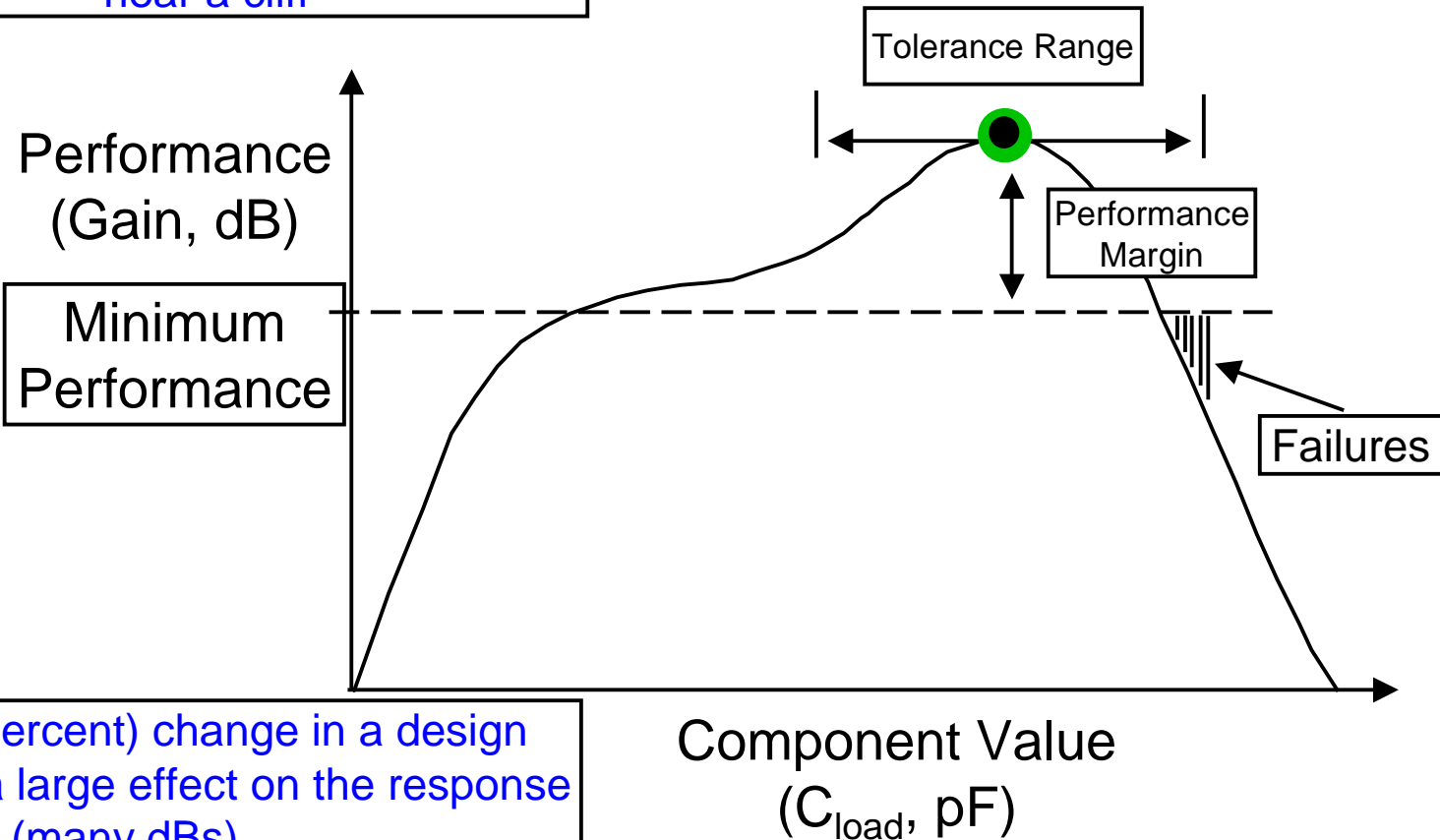
	Included in design	Not included in design
Known effects	<ul style="list-style-type: none">-ideal elements-input match-output match-bias network	<ul style="list-style-type: none">-bends-non-ideal bias components
Unknown effects	<ul style="list-style-type: none">-vias-library parts-measured parts-tees & steps-interactions	Results Matching



Things discovered in the matching step should be added to the circuit design

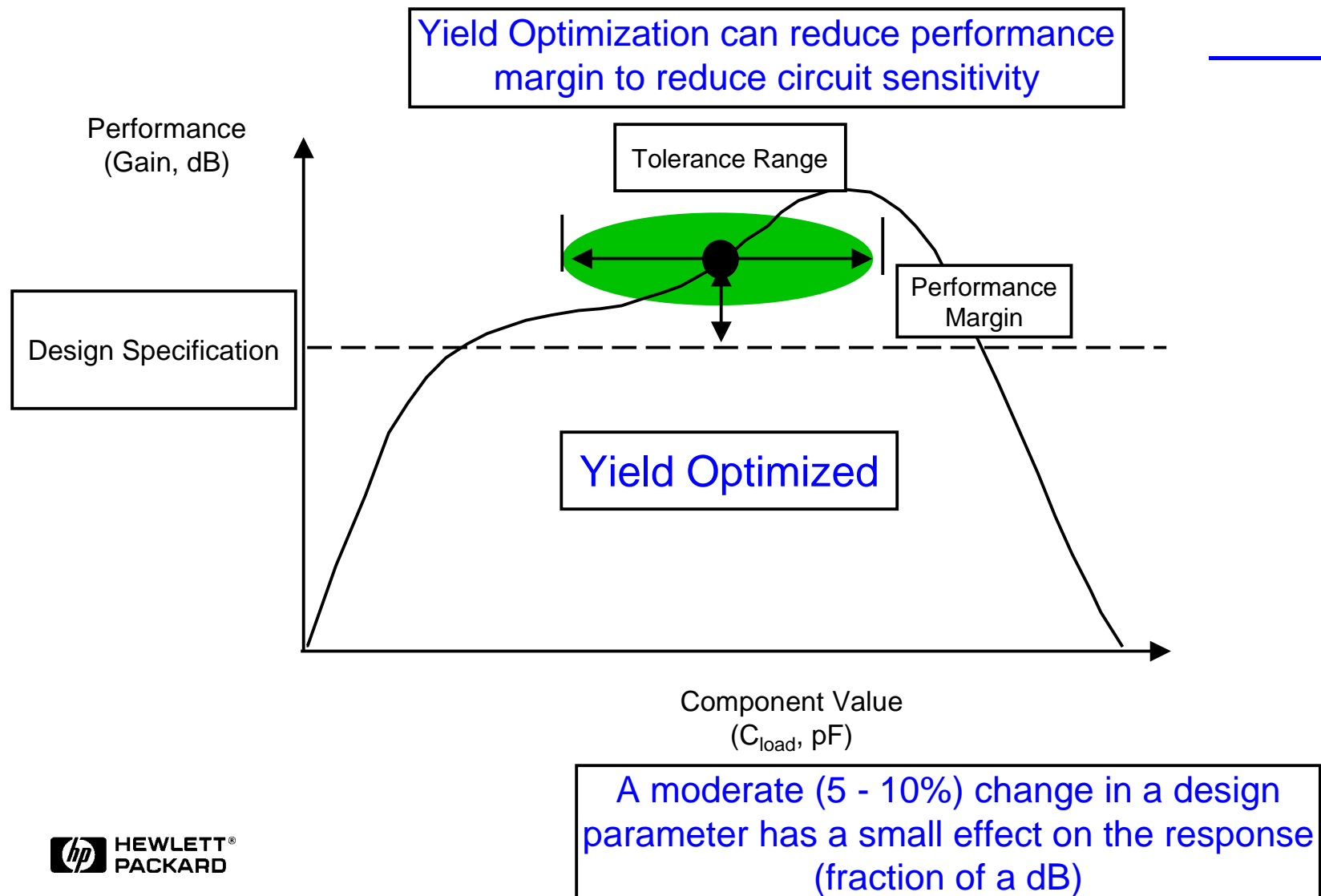
Performance Optimization Weakness

Maximum performance margin can be near a cliff



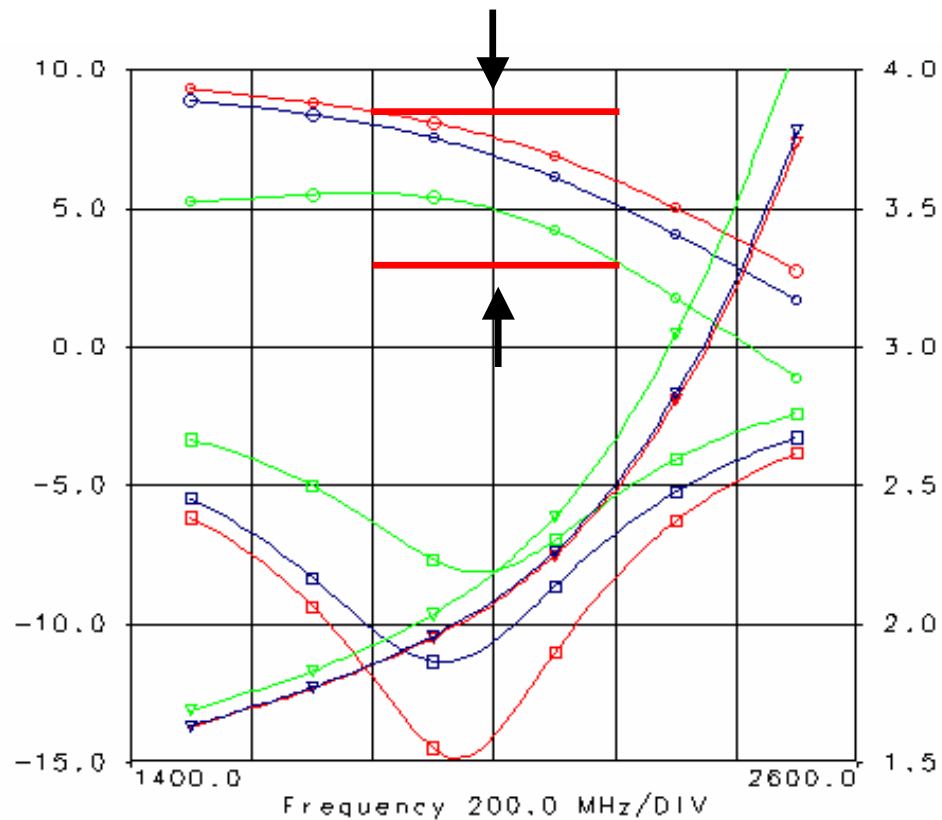
A small (few percent) change in a design parameter has a large effect on the response (many dBs)

Yield Optimized Value



Yield Analysis

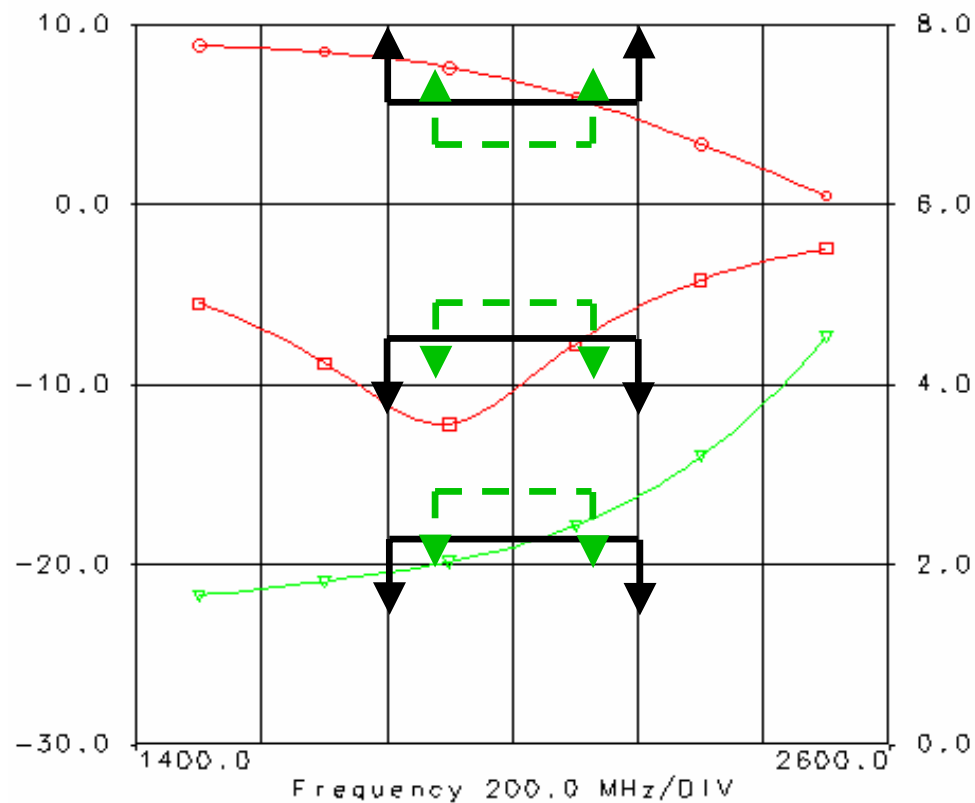
The Effect of Manufacturing Tolerances



When values vary within tolerance, performance can degrade significantly!

Optimization Goals

Performance vs. Yield



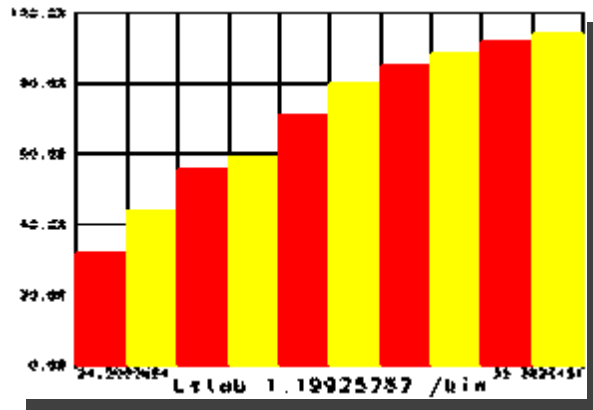
— performance optimization goals

- - - yield optimization goals

Yield Optimization Goals can be less stringent, no longer need to add performance margin.

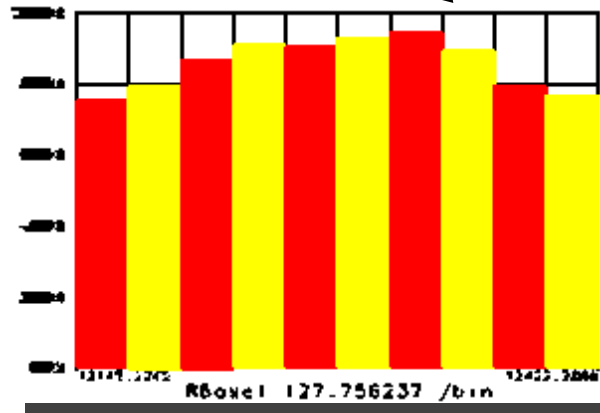
Sensitivity Histograms

Yield



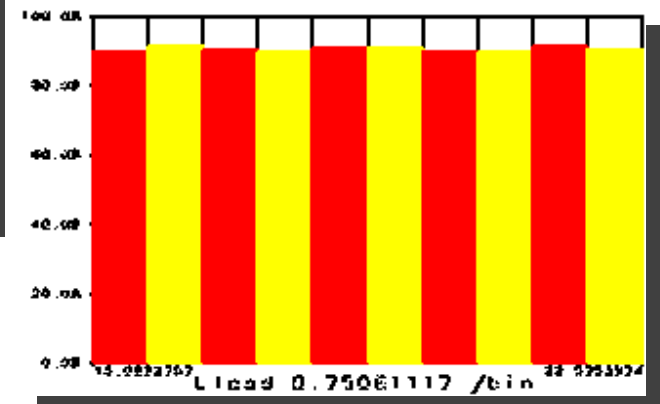
Move Design Center to the Right

Yield vs. Component Value



Nominal Value is Centered,
Tolerance too Wide

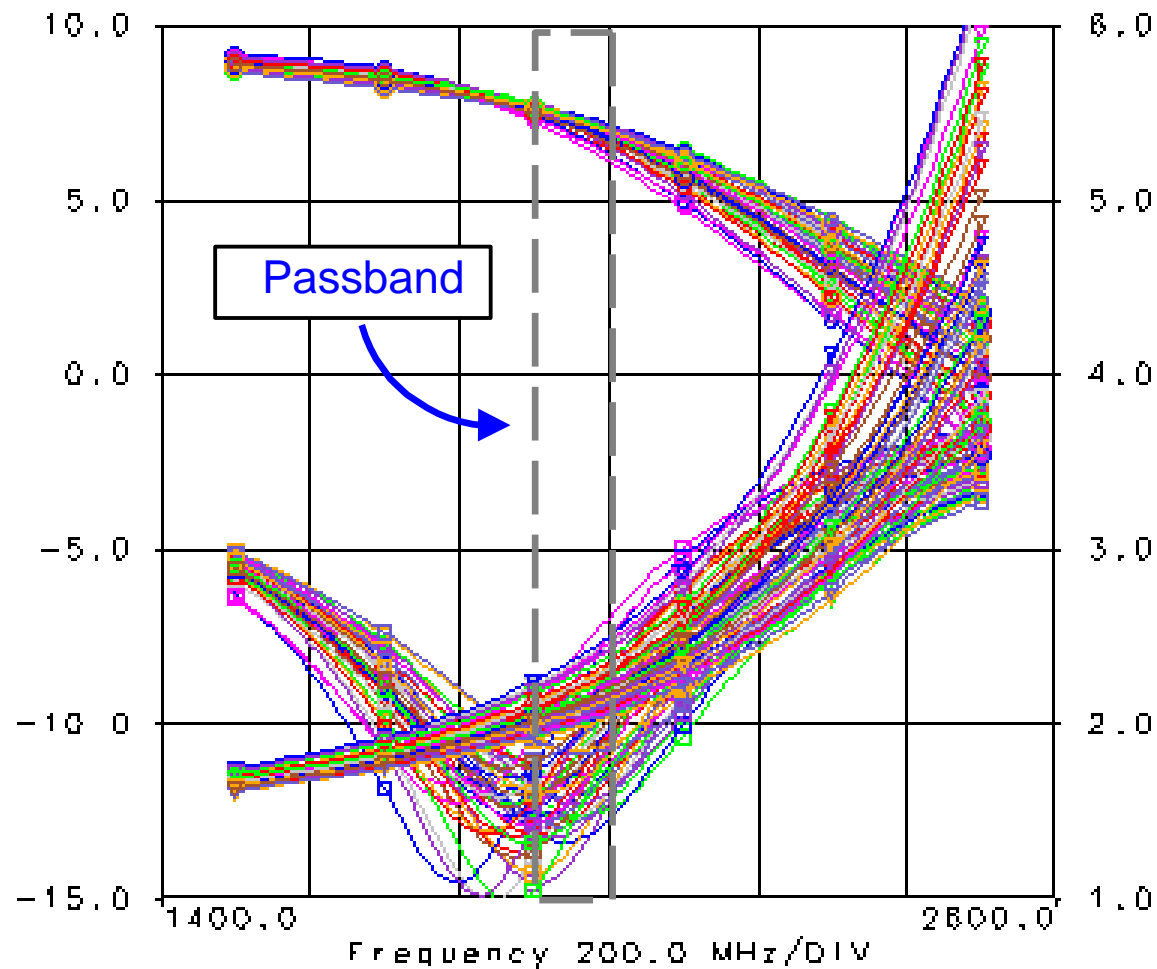
If the component's value were held to just this bin's value, the circuit's overall yield would be 95% instead of just 84%



Nominal Value is Centered,
Tolerance OK
or Perhaps too Narrow

LNA Example

Yield with 10% Tolerances



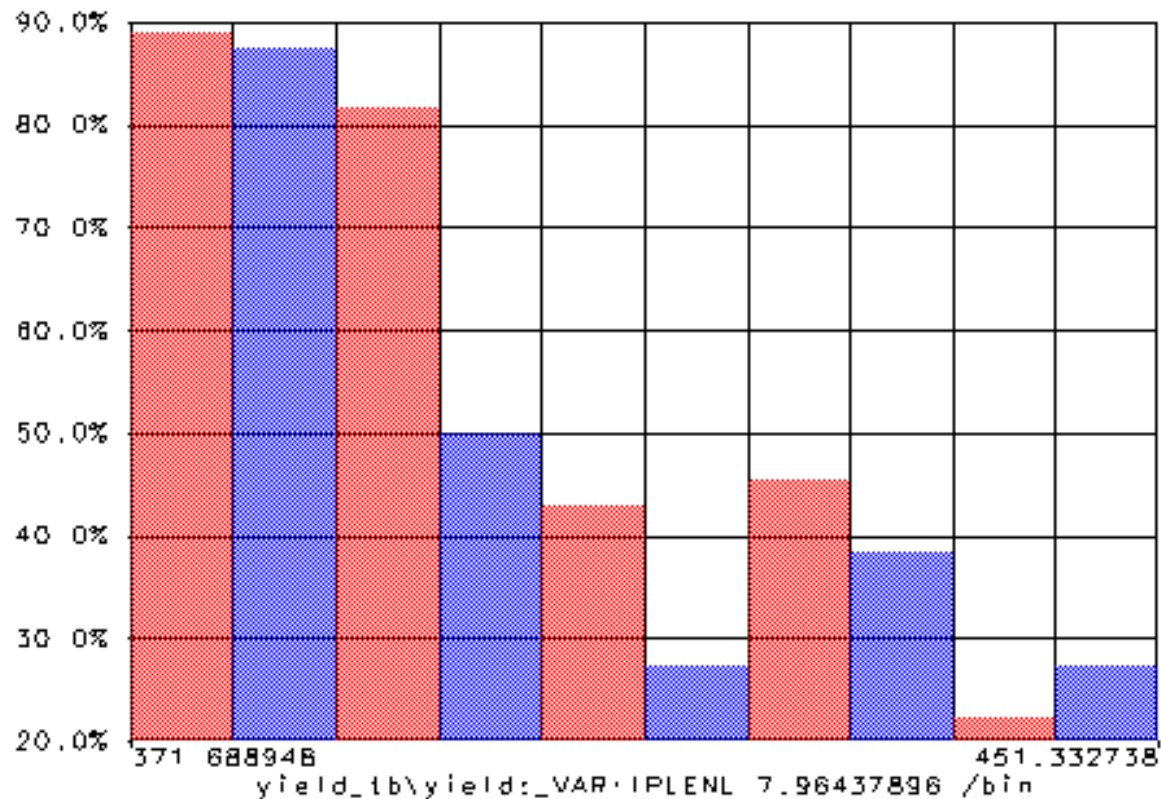
54% yield

Optimization Goals:
Gain > 6.5 dB
S11 < -10
NF < 2.5

Tolerance: 10%

LNA Example Sensitivity Histograms

yield_1b
Yield
Yield



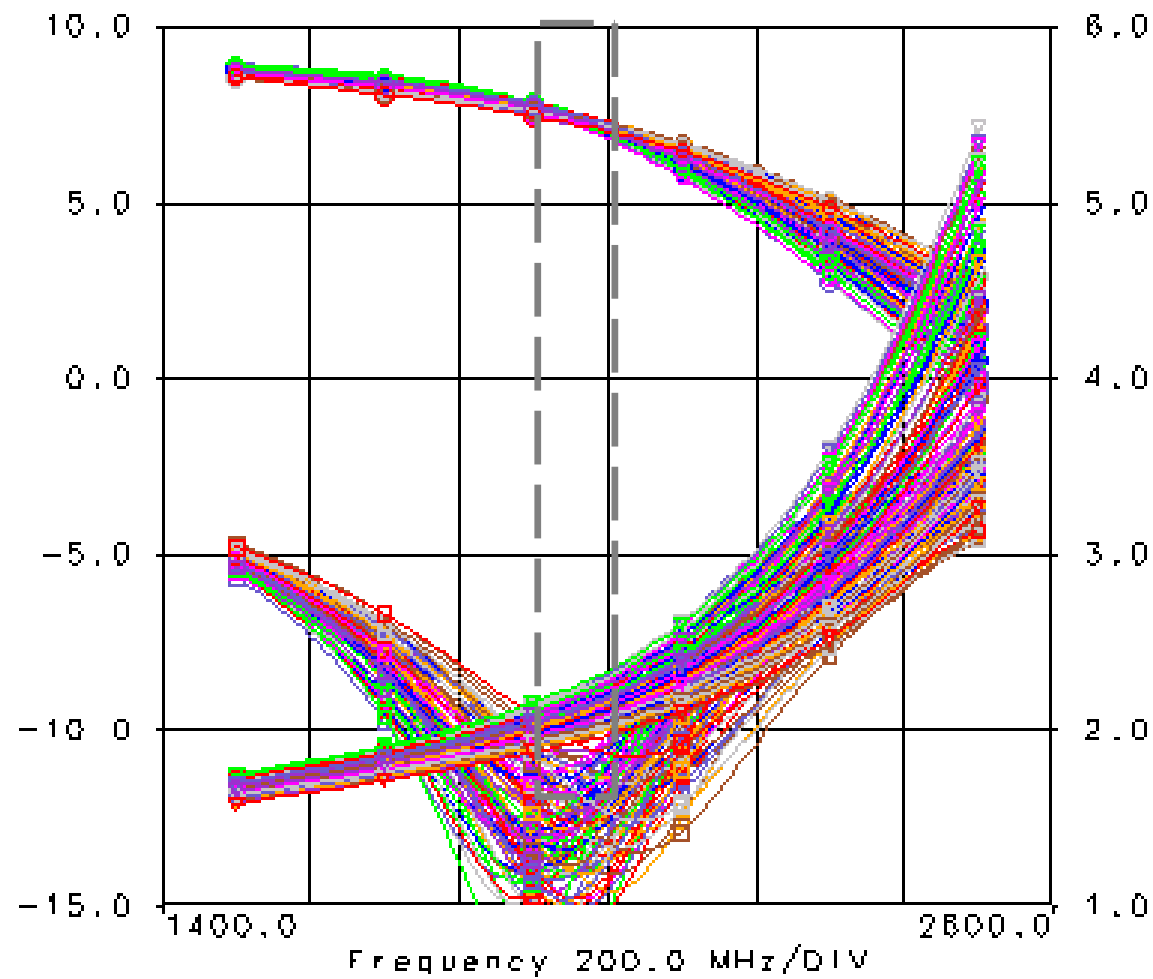
Variable = IPLENL

Yield would increase if
we chose a larger
nominal value

Yield Sensitivity

LNA Example

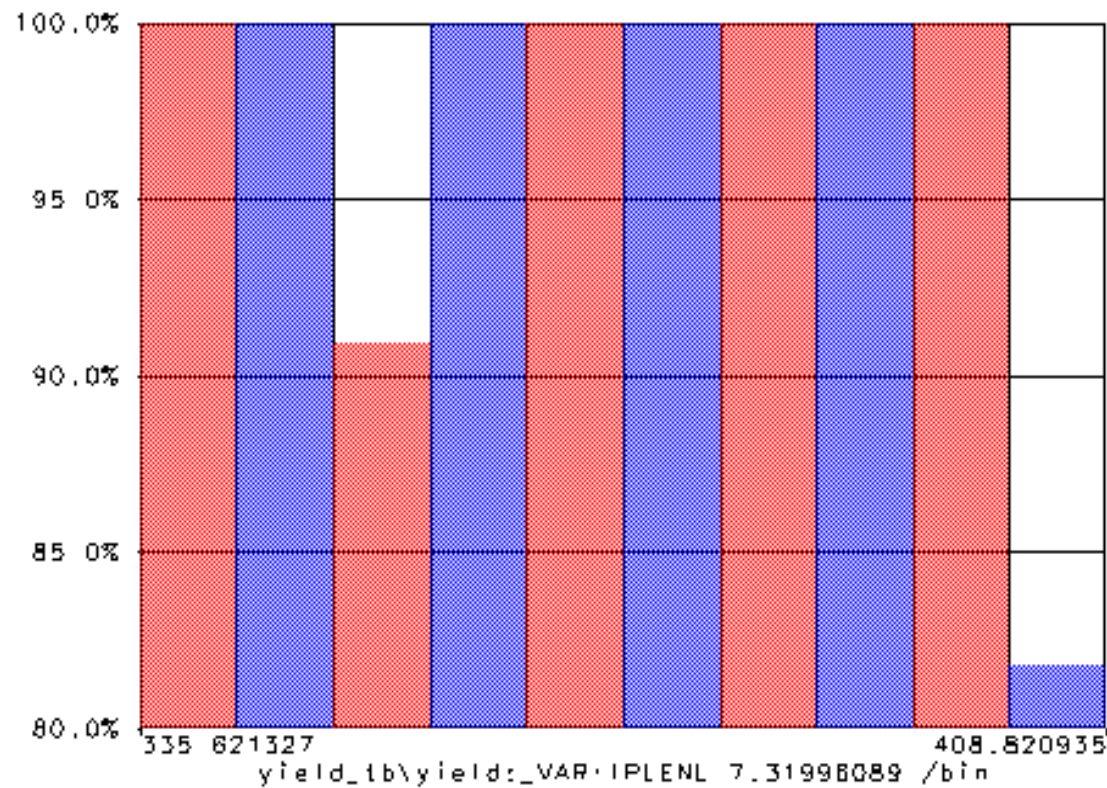
Yield After Design Centering



98% yield

Sensitivity Histogram After Design Centering

yield_tb
Yield
Yield



98% yield

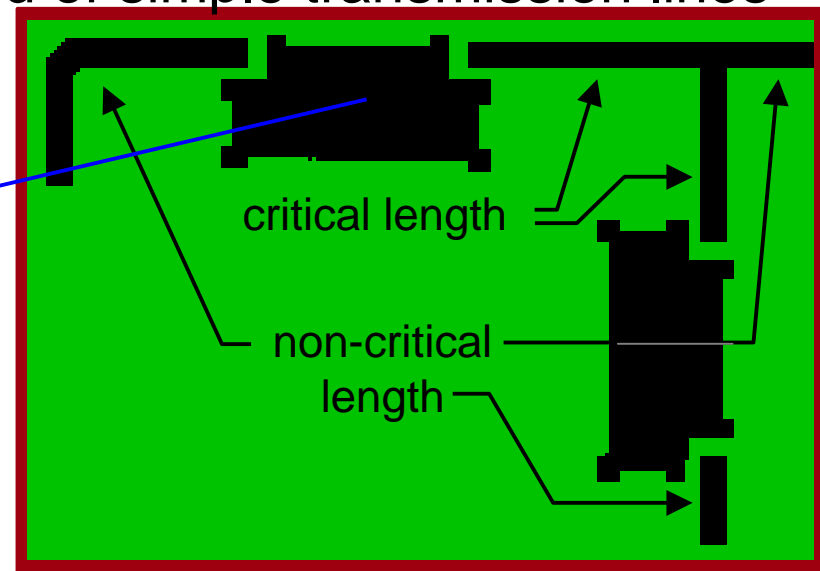
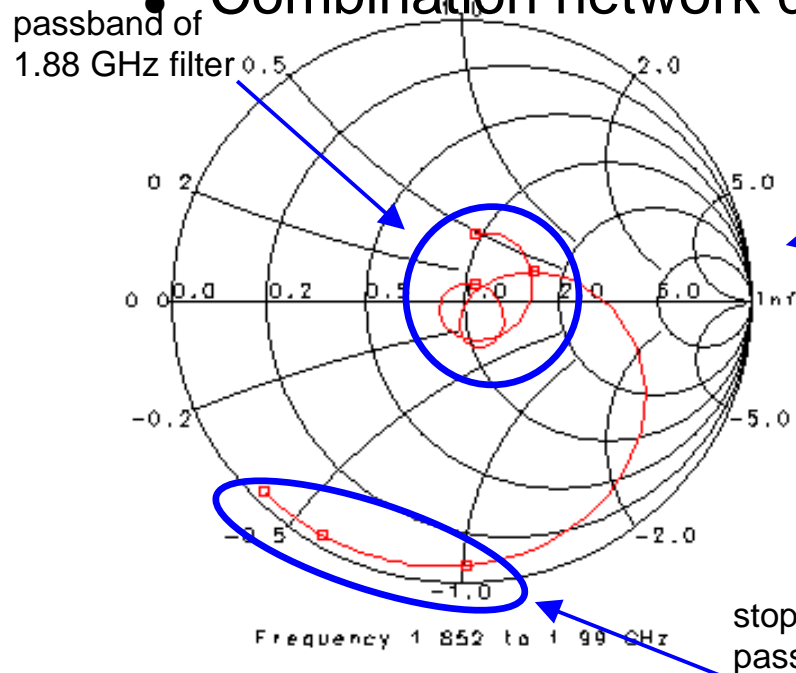
Variable = IPLENL

Yield Sensitivity



Duplexer Design

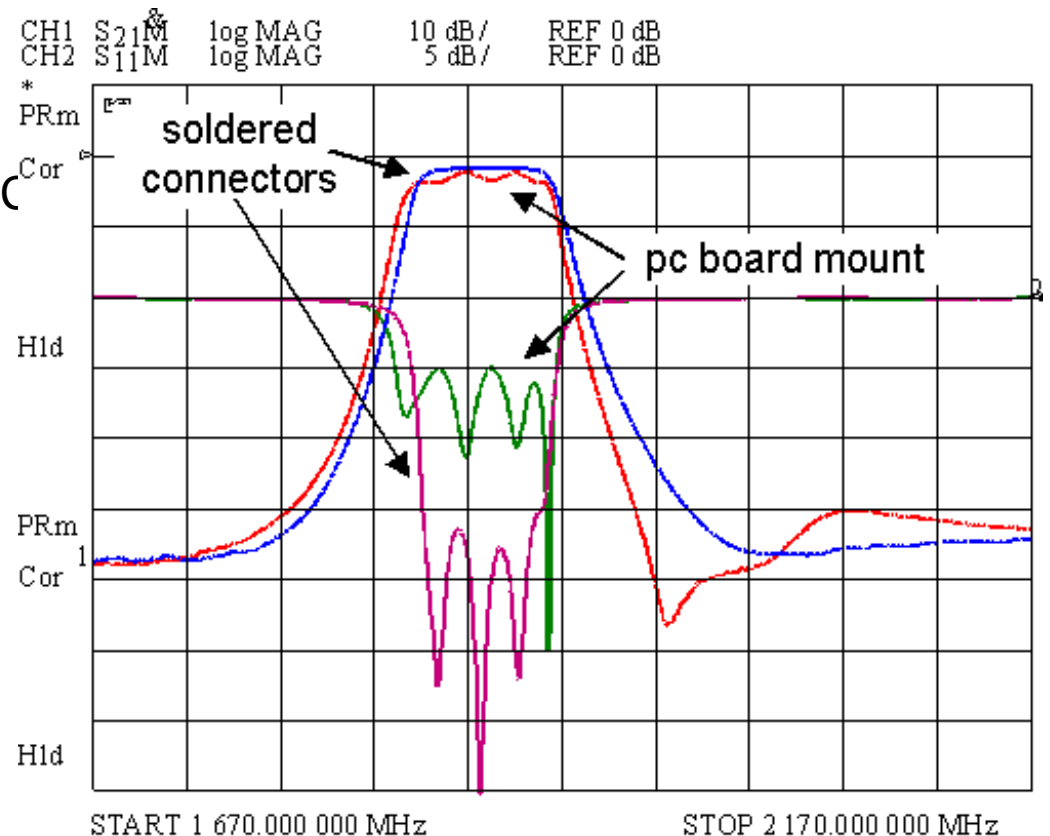
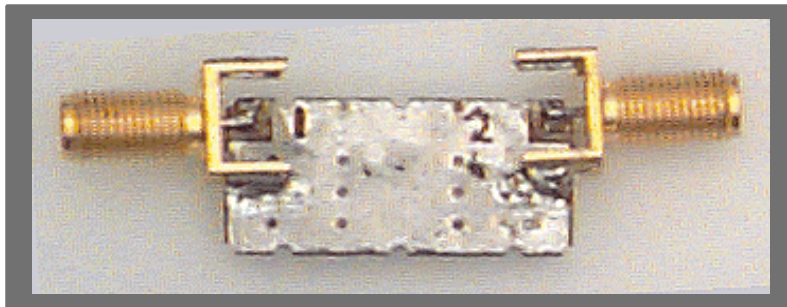
- Duplexer constructed of two separate bandpass filters
- Stopband of one filter must not interfere with passband of other filter (and vice versa)
- Each filter was measured, then combination network was designed and simulated using S-parameter data files
- Combination network consisted of simple transmission lines



stopband of 1.88 GHz filter at
passband of 1.96 GHz filter

Duplexer Filter Measurements

- First attempt: used PC board fixture
 - Results had a lot of ripple and loss
 - Blamed on poor launches and non-50 Ω transmission lines
- Second attempt: soldered connectors directly to filter
 - Response looked good
 - Will filter measure same on final PC board?



Duplexer's Measured Performance

