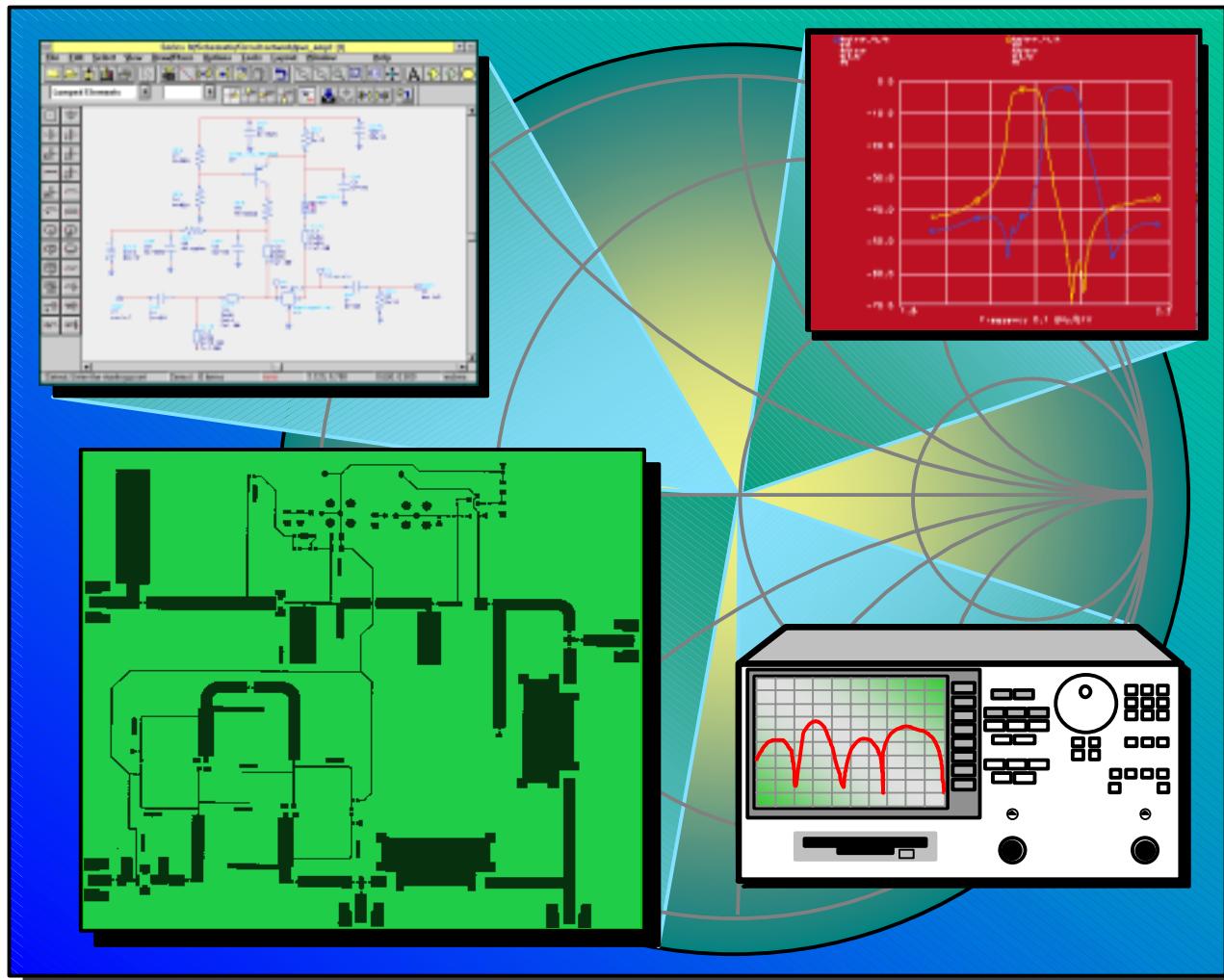


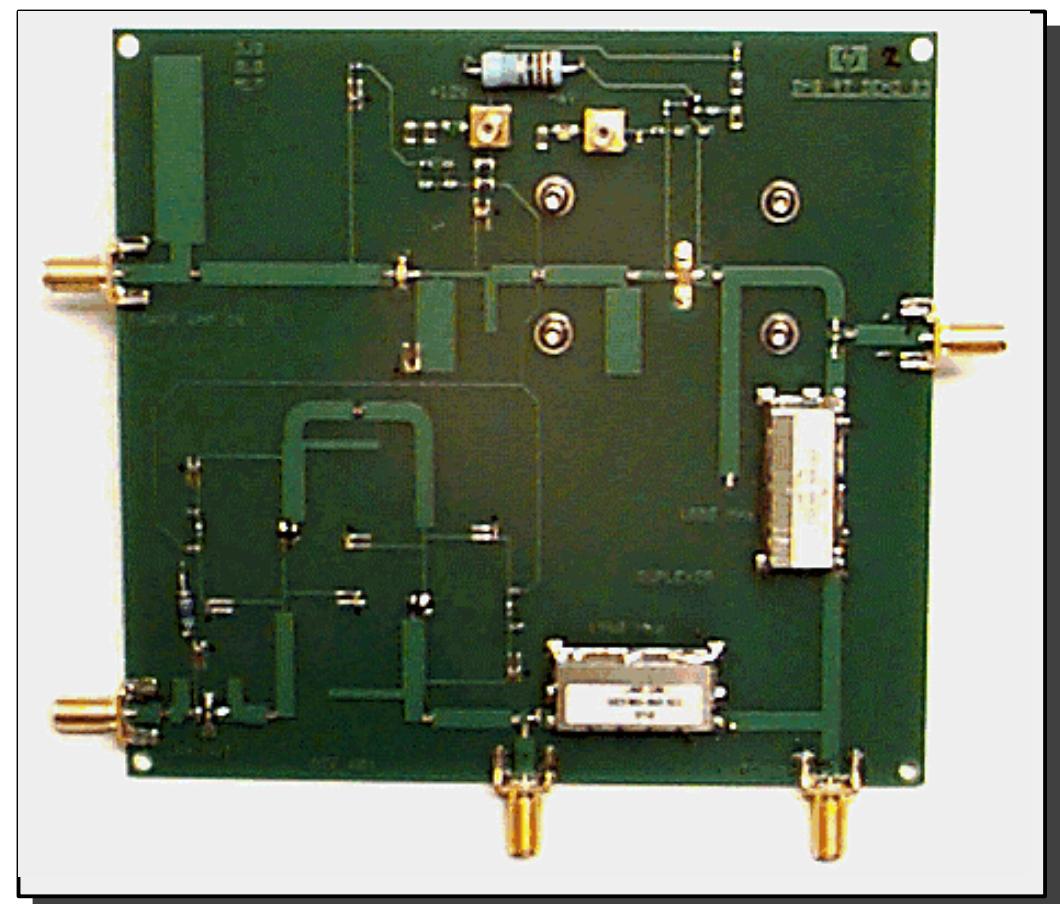
# *HP RF Design and Measurement Seminar*



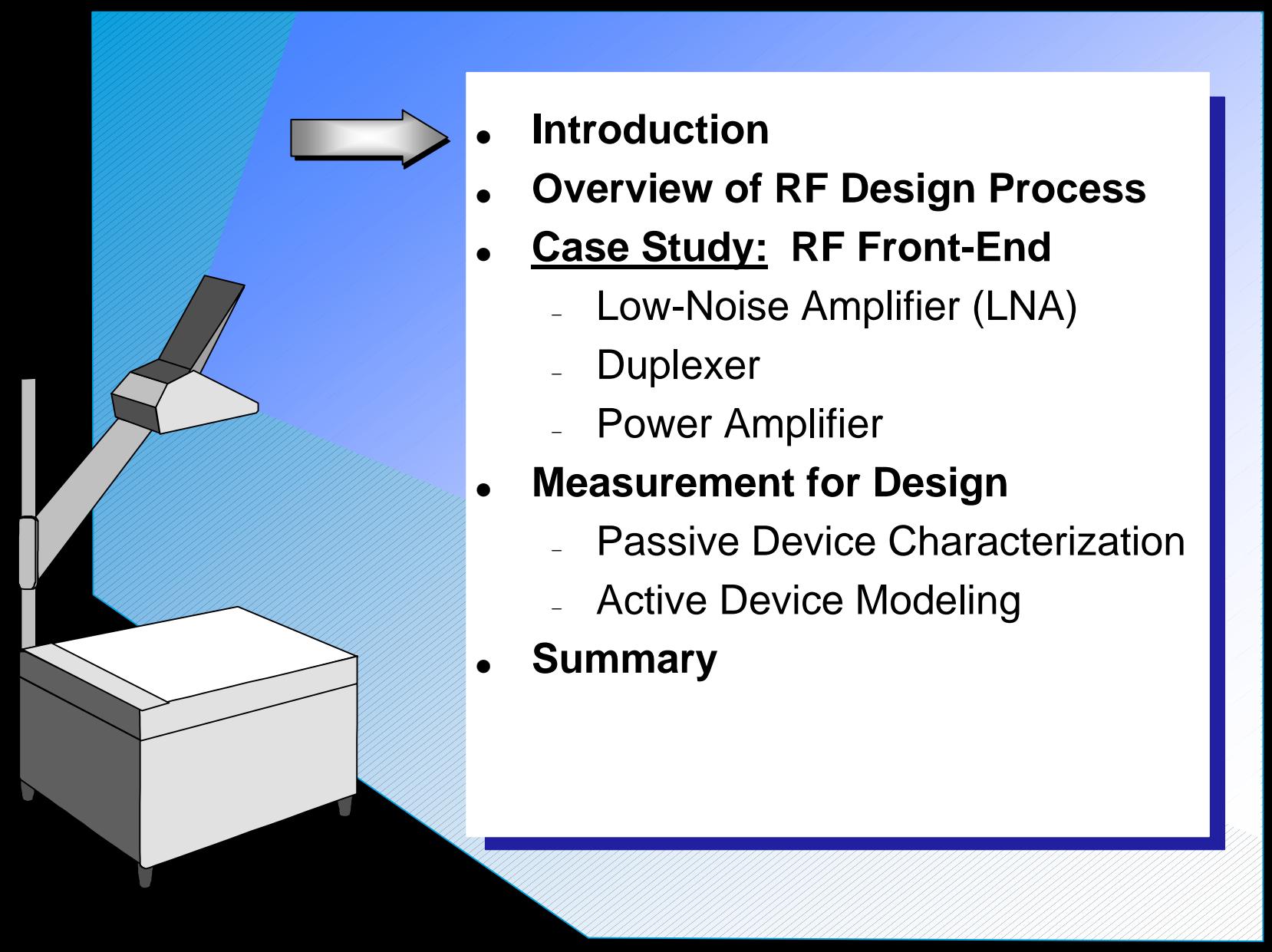
**Creators:**  
*David Ballo*  
*Andy Potter*  
*Boyd Shaw*  
*My Le Truong*  
*Joe Civello*  
*Ed Henicle*  
*Sara Meszaros*

# Goals of the Seminar

- Introduce new engineers to the modern RF design process
- Document predictive RF design process
- Focus on design methodology, not button pushing
- Provide practical design tips based on our case study



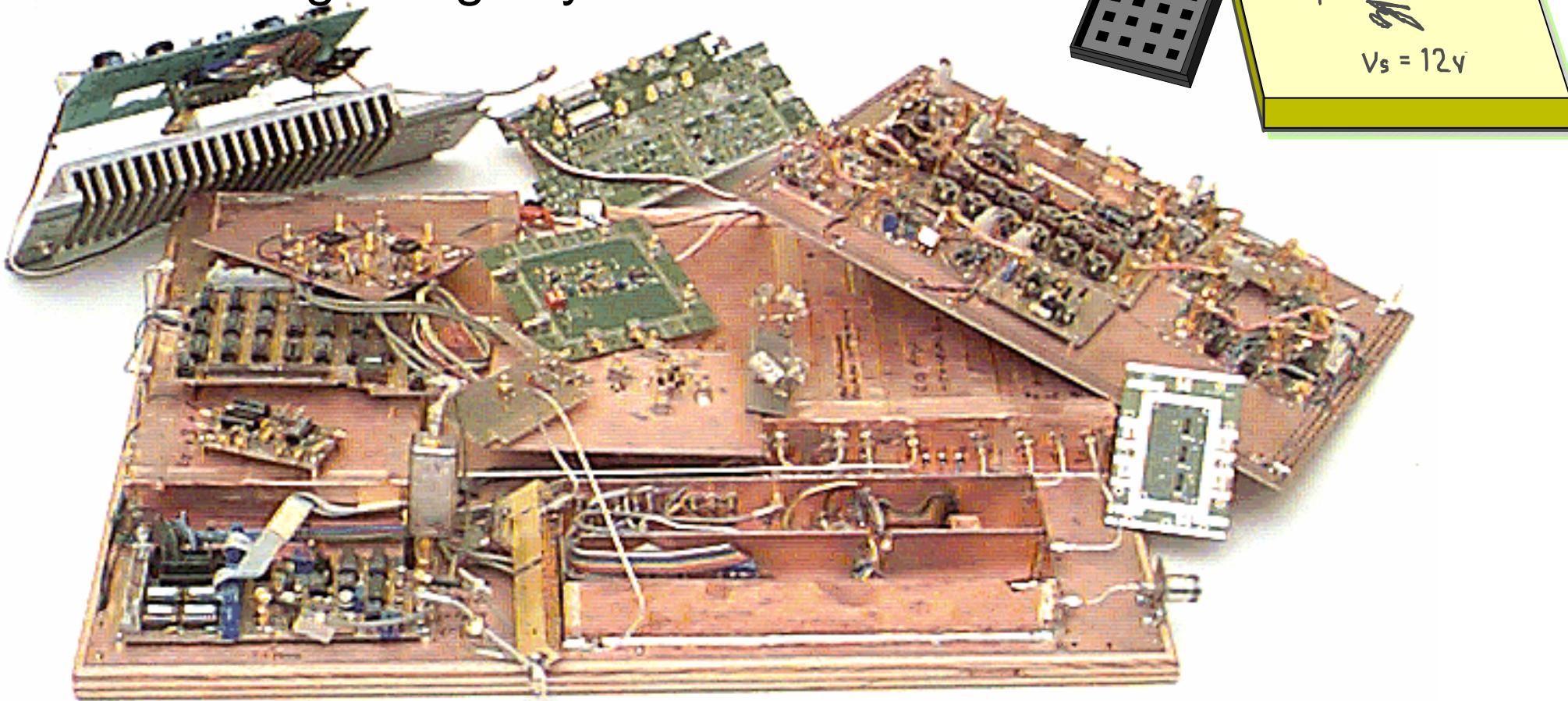
# Agenda



- **Introduction**
- **Overview of RF Design Process**
- **Case Study: RF Front-End**
  - Low-Noise Amplifier (LNA)
  - Duplexer
  - Power Amplifier
- **Measurement for Design**
  - Passive Device Characterization
  - Active Device Modeling
- **Summary**

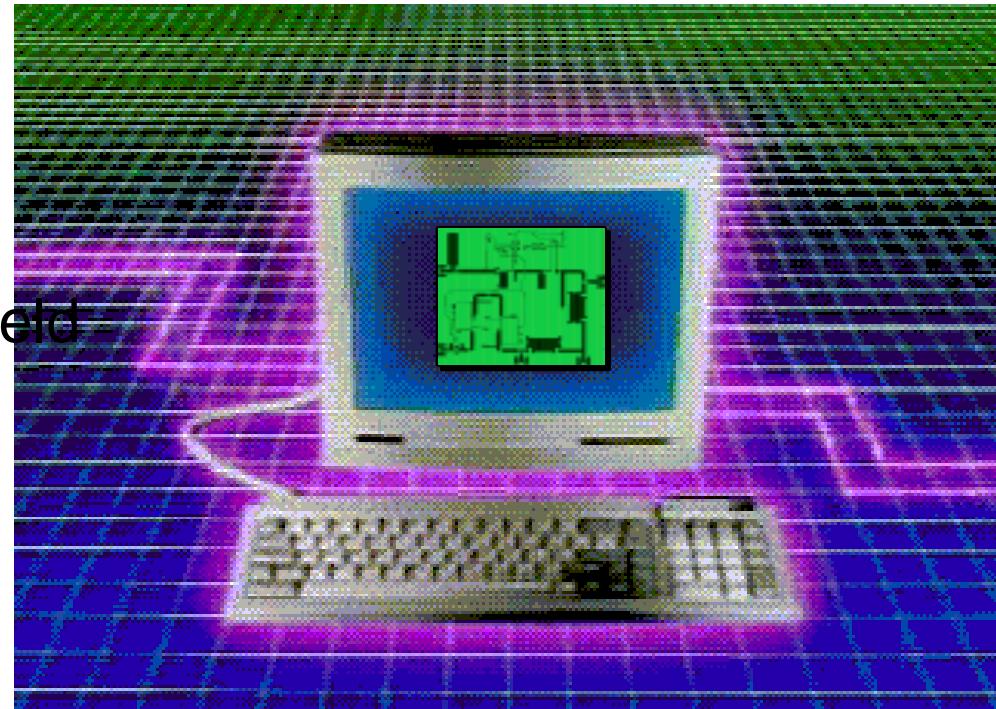
# Traditional RF Design Process

- Paper, pencil, calculator
- Many board turns (cut and try)
- Long design cycles

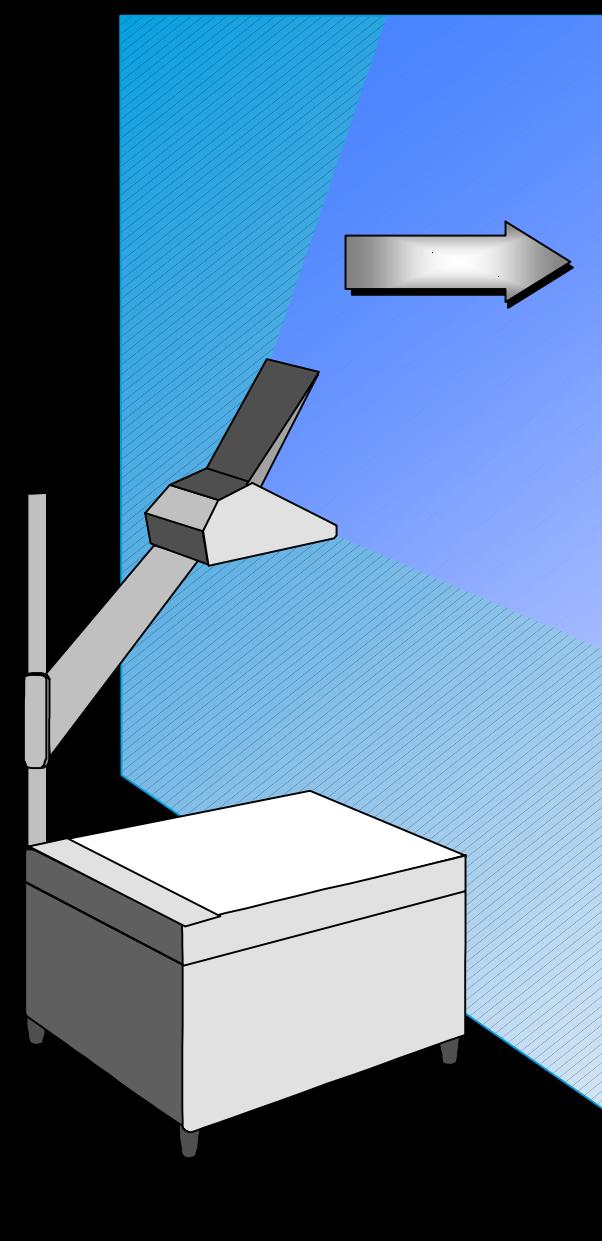


# Modern, Predictive RF Design Process

- Combination of:
  - EDA (electronic design automation) software
  - Measurement equipment (e.g., network & signal analyzers)
- Design iterations now performed via software
- Fewer board turns (faster time to market)
- Accurate circuit performance - minimize over engineering
- Improve manufacturability with yield analysis and optimization



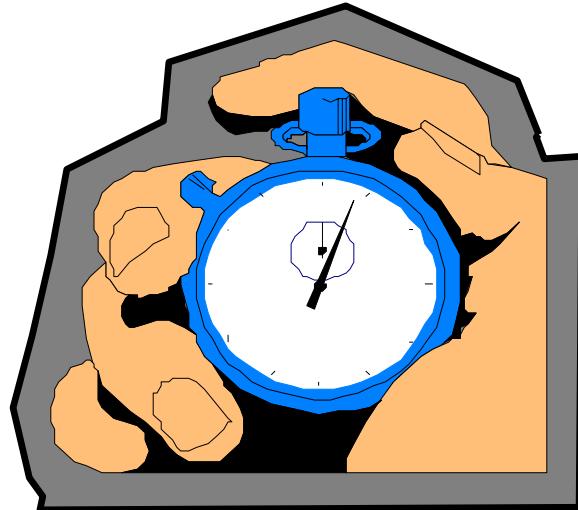
# Agenda



- **Introduction**
- **Overview of RF Design Process**
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  - Passive Device Characterization
  - Active Device Modeling
- **Summary**

# Three Critical Design Considerations

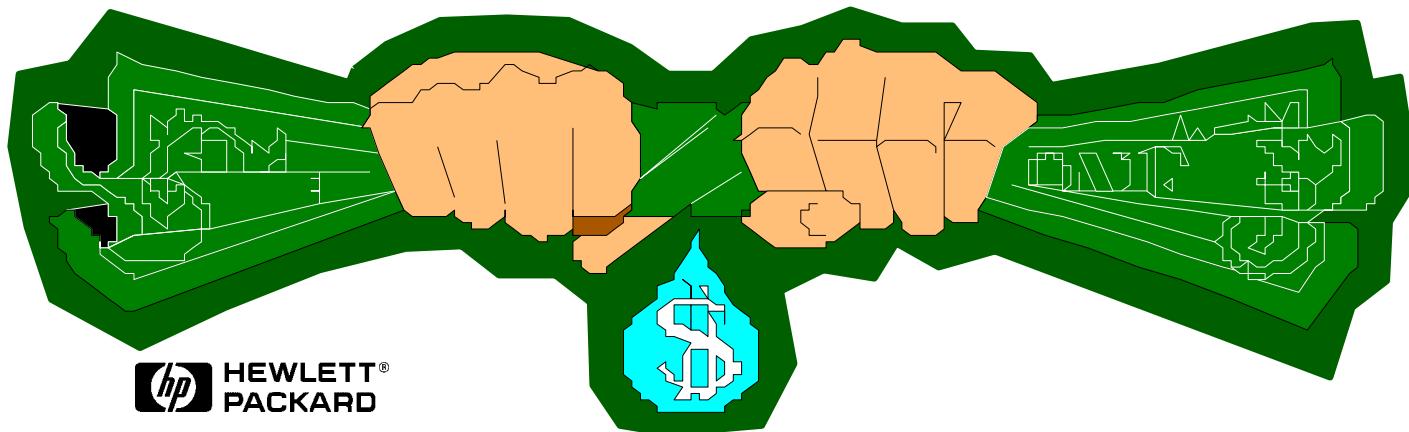
Time to Market



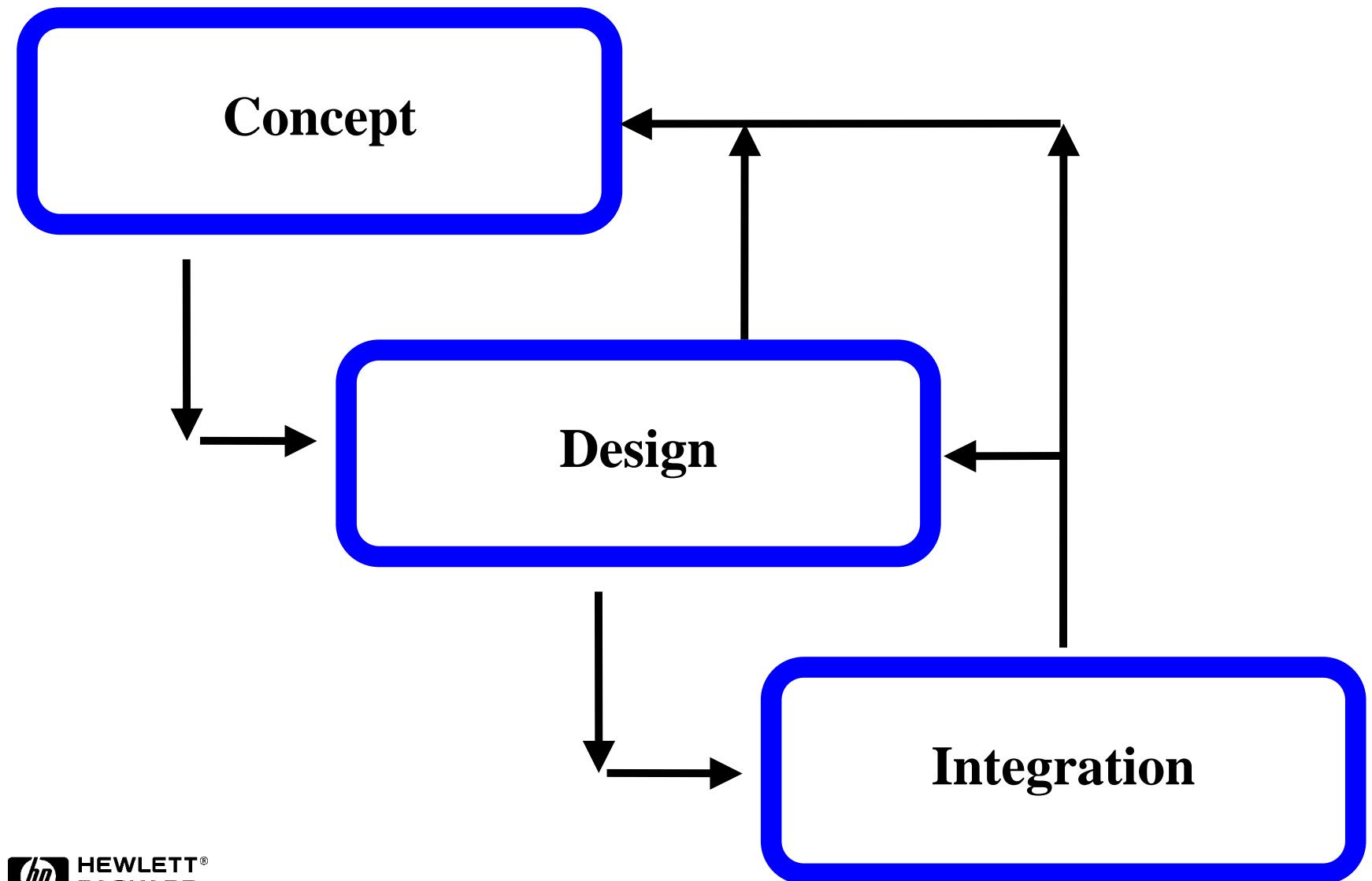
Performance



Cost



# General RF Design Process

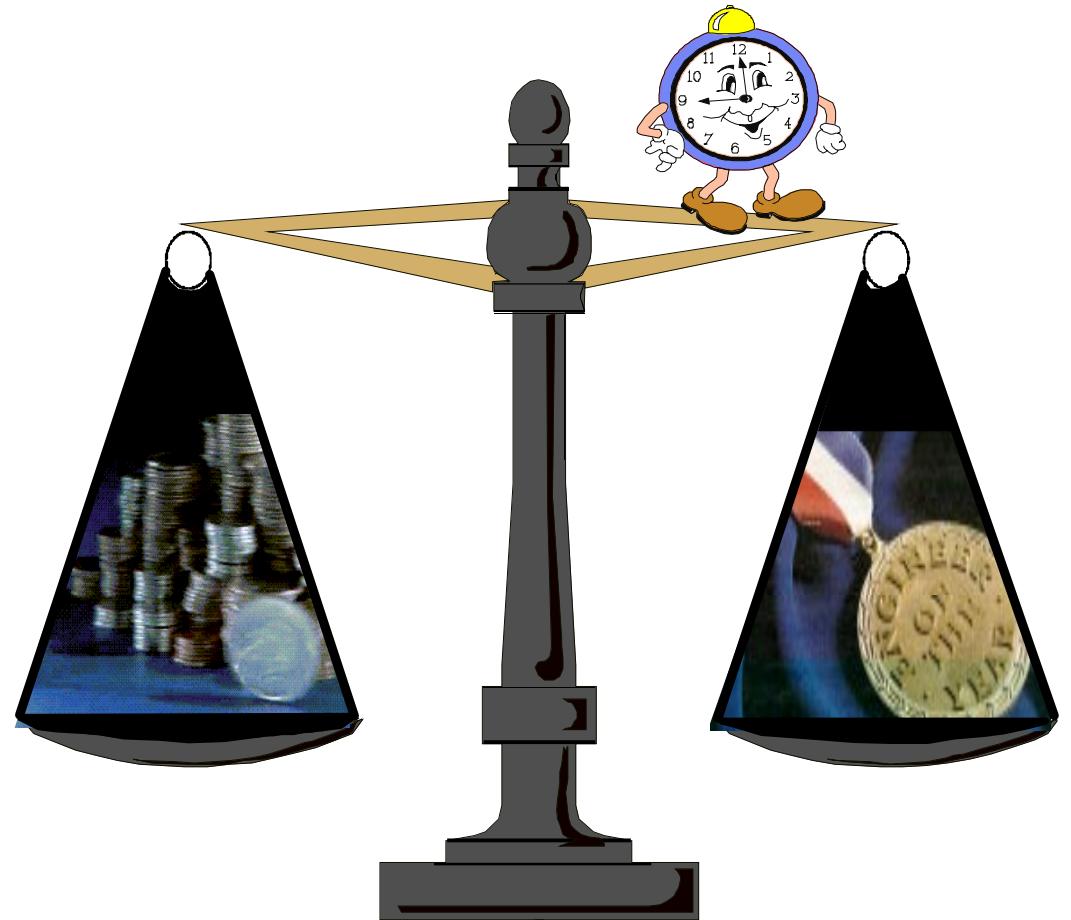


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# Concept: System Design\Analysis\Partition

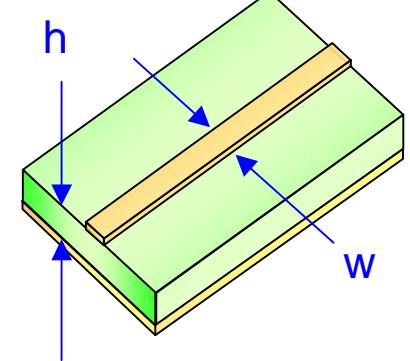
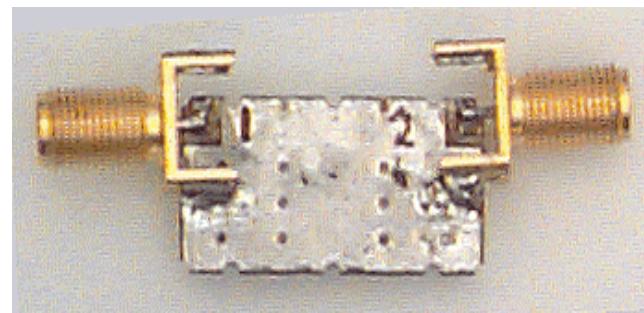
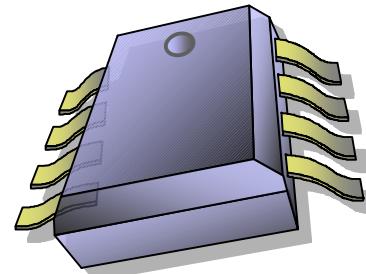
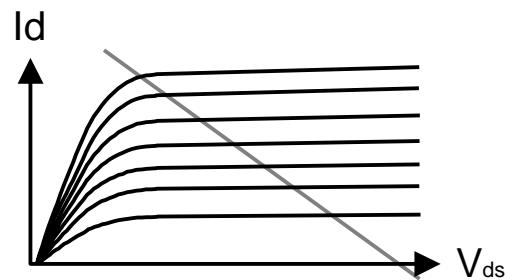
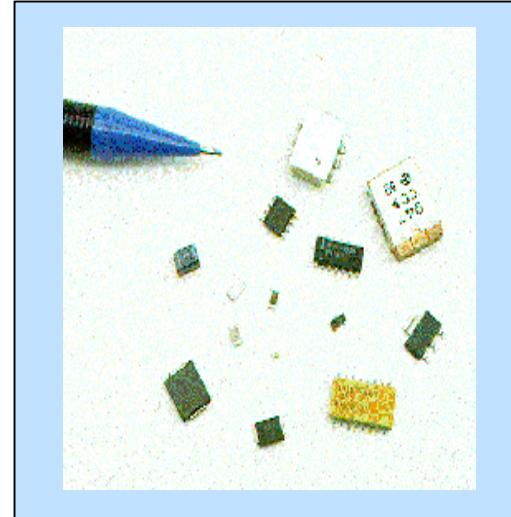
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- Assess goals
- Set priorities
- Explore possible system configuration
- Design partitioning
- Allocate circuit specifications



# Circuit Level Design

- Explore possible circuit topologies
- Investigate and select components
- Make build vs. buy decisions
- Determine whether desired circuit Specifications are realizable
- Verify system performance

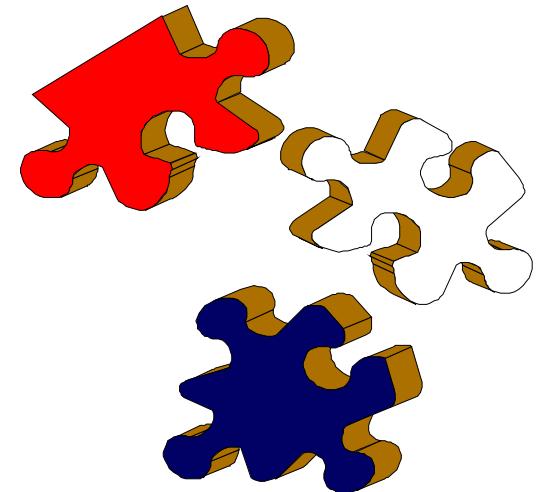


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# Integration

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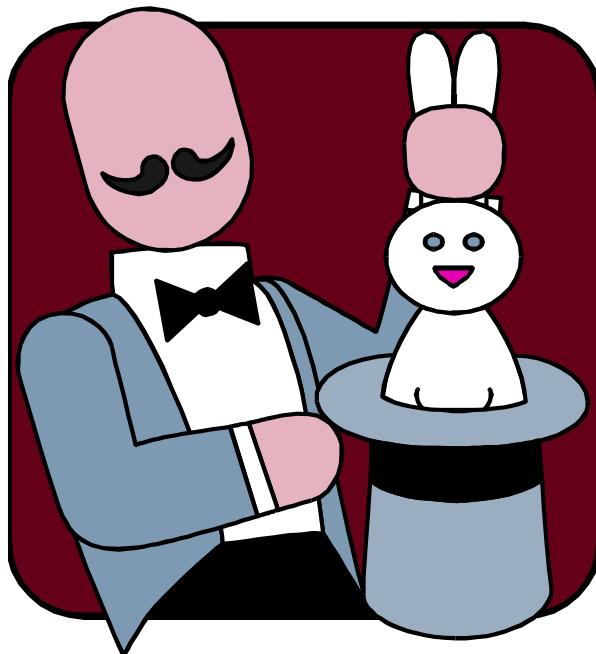
- Combine individual circuits
- Troubleshoot
  - System redesign, as needed
  - Circuit redesign
  - Circuit reallocation
  - System reconfiguration
- Modify system specification, as needed
- Re-define project definition, as needed



---

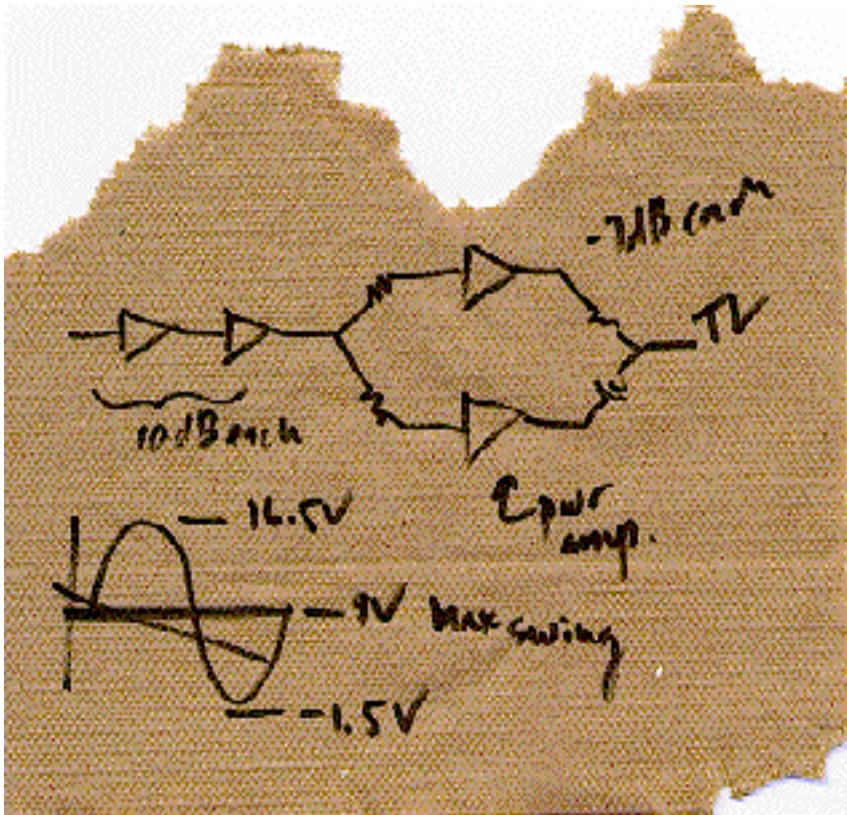
# The Traditional Design Process

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# Concept: System Design/Analysis/Partition

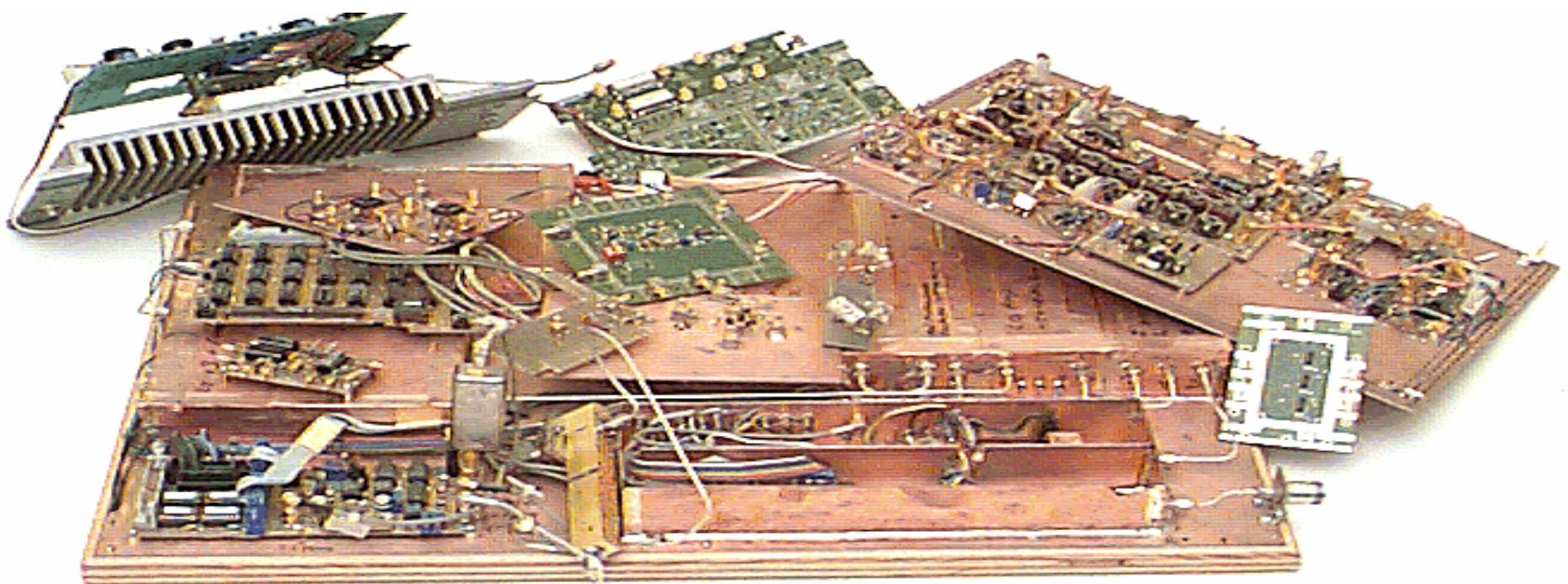


- Understand needs and goals
- Paper study
  - Prone to errors
  - Incomplete system analysis
  - Difficult to analyze circuit interactions

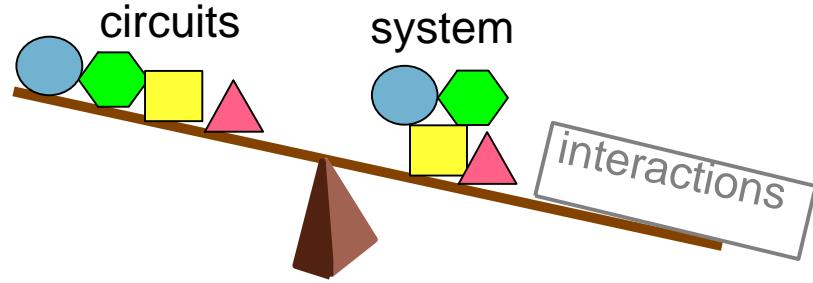


# Circuit Level Design

- Reliance on physical breadboards (prototypes)
- Trial-and-error circuit design (cut & try)
- Difficult to verify circuit's performance on system level
- Difficult to predict interactions & manufacturing yield
- Expensive & time consuming!!!



# Integration & Test



*Once integrated, system =  
 $\sum$  circuit + circuit interactions*

- Trouble shooting
  - System level
  - Circuit level
- Little flexibility
- Expensive changes
- Inefficient process

oscillation!

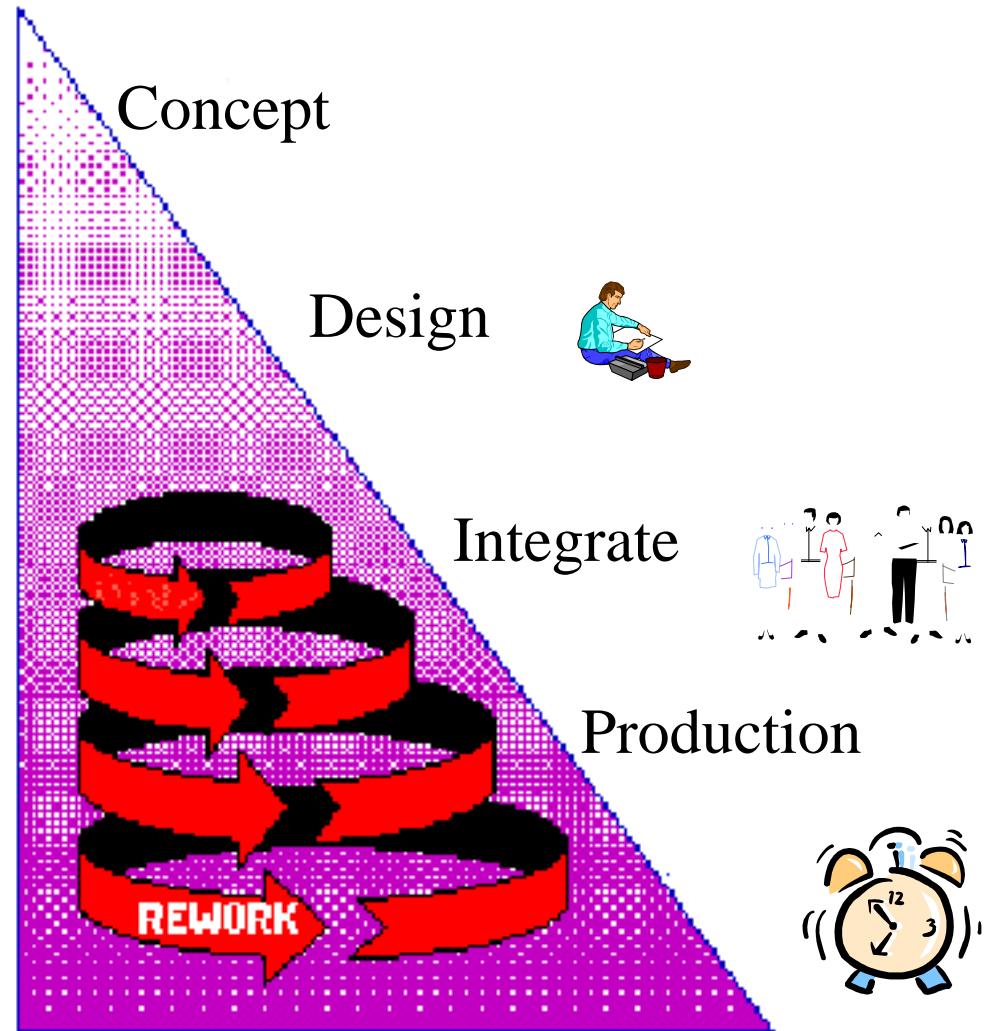
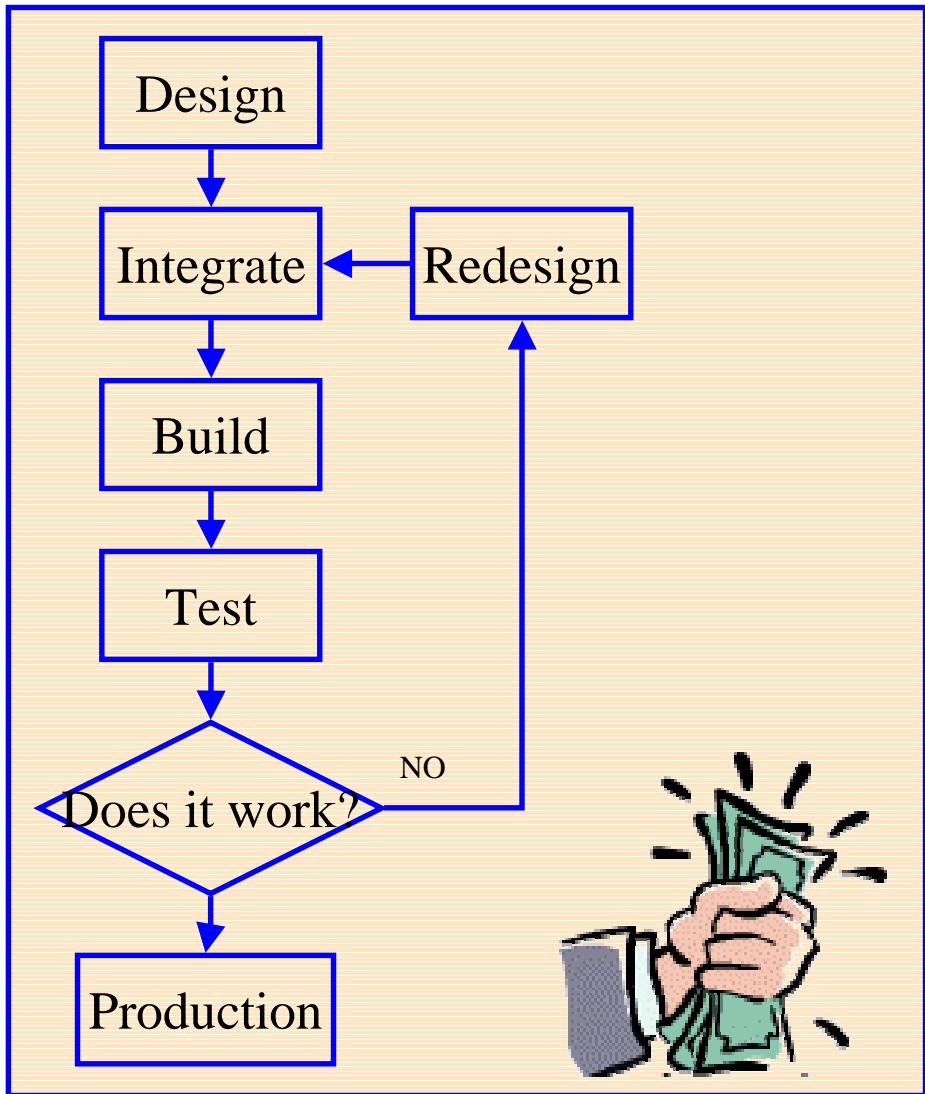


spurs!





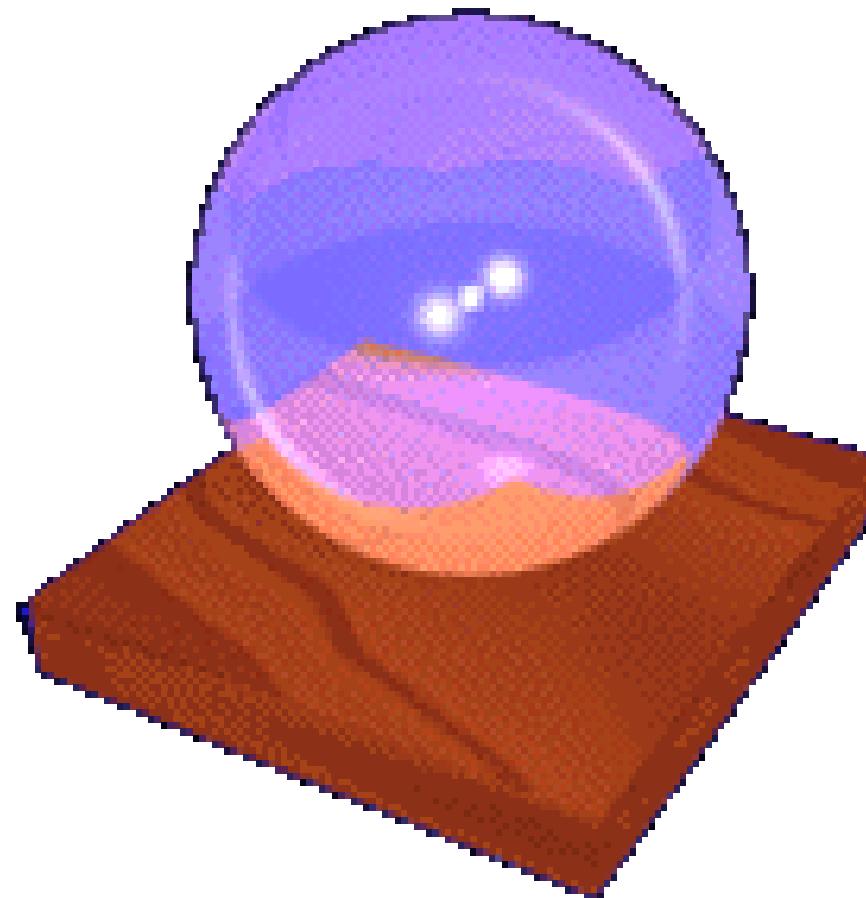
# Traditional Design Process



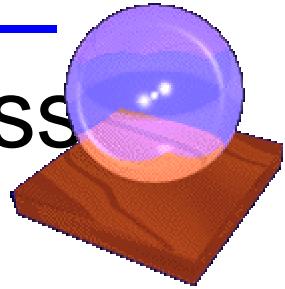
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# Modern, Predictive RF Design Process

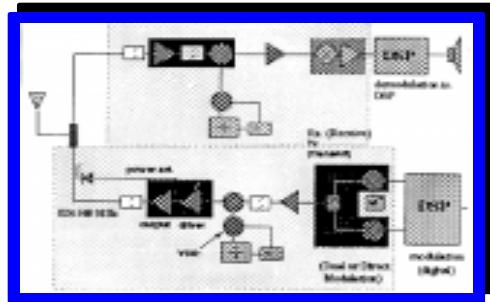
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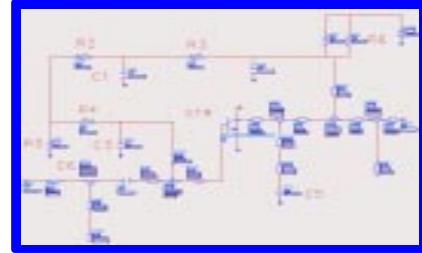
# Modern, Predictive RF Design Process



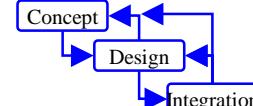
*Combine test equipment and EDA software for fast, efficient design!*



Concept



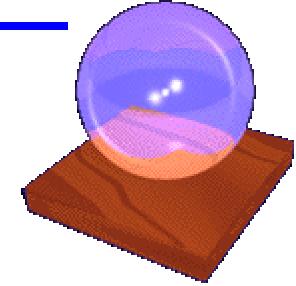
Design



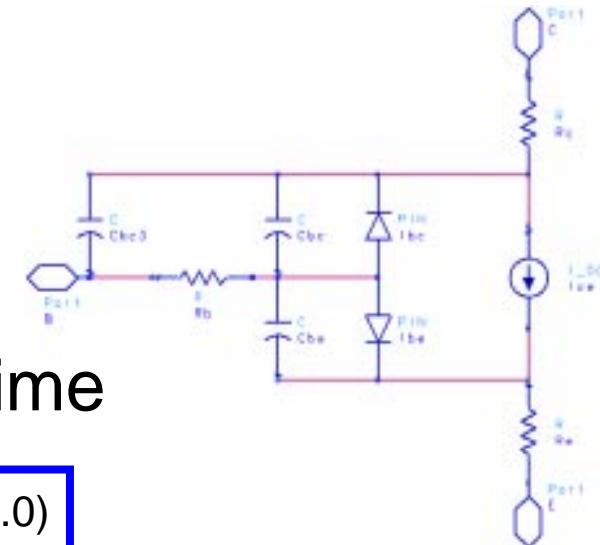
Integration



# Investment in Models



- Dedicate modeling team
- Use available parts libraries
- Measure individual parts
  - Different operating conditions
  - Improve individual parts models with time



$$I_{be} = (I_{Bbif} \exp(V_{be}/N_{bf}V_T) - 1.0) + I_{se} \exp(V_{be}/(N_{se}V_t) - 1.0)$$

A standard electronic symbol for a transistor, showing a vertical line with a diagonal line extending from its top and another line extending from its bottom.

```

BJT_Model
BJTM2
NPN=yes      B=      C=      Rce
PNP=no       Ikr=    Vc=      Kfe
Bf=          Isc=    Mje=     Af=
Ikf=         Nce=    Xcjc=   Kbm
Ise=         Vorm=   Fc=      Ab=
Nee=         Nre=    Cje=    Fb=
Vaf=         Tr=     Vje=    Ffe=
Nf=          Eg=     Mje=    Lateral=no
Tf=          Is=     Cjs=    AllParams=
Xtf=         Img=    Vjs=
Vtf=         Xti=    Mje=
Itf=         Tnem=   Rb=
Ptf=         Nke=    Irb=
Xtb=         Iss=    Rbm=
Approxqb=yes Nse=    Re=

```

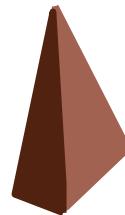
```
!Freq.[Hz] MagS11[dB] PhaseS11[DEG] MagS21[dB] PhaseS21[DEG] MagS12[dB] PhaseS12[DEG]
300000 -5.986E-07 -1.151E-02 -7.394E+01 8.997E+01 -7.394E+01 8.997E+01 -5.986E-07 -1.151E-02
315229 -6.384E-07 -1.210E-02 -7.351E+01 8.997E+01 -7.351E+01 8.997E+01 -6.384E-07 -1.210E-02
331231 -6.812E-07 -1.271E-02 -7.308E+01 8.997E+01 -7.308E+01 8.997E+01 -6.812E-07 -1.271E-02
348046 -7.273E-07 -1.336E-02 -7.265E+01 8.997E+01 -7.265E+01 8.997E+01 -7.273E-07 -1.336E-02
365714 -7.769E-07 -1.403E-02 -7.222E+01 8.997E+01 -7.222E+01 8.997E+01 -7.769E-07 -1.403E-02
384279 -8.303E-07 -1.475E-02 -7.179E+01 8.997E+01 -7.179E+01 8.997E+01 -8.303E-07 -1.475E-02
403787 -8.879E-07 -1.550E-02 -7.136E+01 8.997E+01 -7.136E+01 8.997E+01 -8.879E-07 -1.550E-02
424285 -9.501E-07 -1.628E-02 -7.093E+01 8.997E+01 -7.093E+01 8.997E+01 -9.501E-07 -1.628E-02
445823 -1.017E-06 -1.711E-02 -7.050E+01 8.997E+01 -7.050E+01 8.997E+01 -1.017E-06 -1.711E-02
468455 -1.090E-06 -1.798E-02 -7.007E+01 8.997E+01 -7.007E+01 8.997E+01 -1.090E-06 -1.798E-02
492235 -1.168E-06 -1.889E-02 -6.964E+01 8.997E+01 -6.964E+01 8.997E+01 -1.168E-06 -1.889E-02
517223 -1.252E-06 -1.985E-02 -6.921E+01 8.997E+01 -6.921E+01 8.997E+01 -1.252E-06 -1.985E-02
543479 -1.344E-06 -2.086E-02 -6.878E+01 8.997E+01 -6.878E+01 8.997E+01 -1.344E-06 -2.086E-02
```

# Concept: System Design/Analysis/Partition



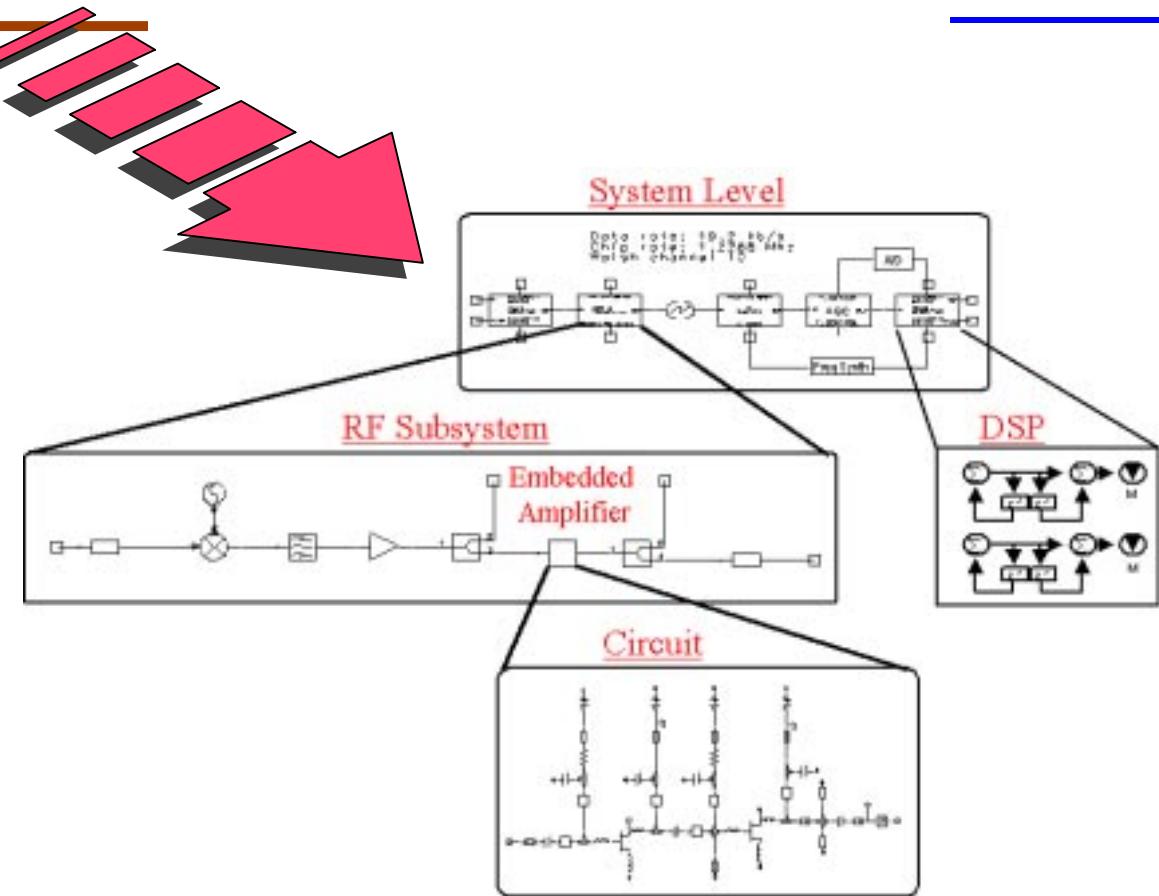
circuits

system



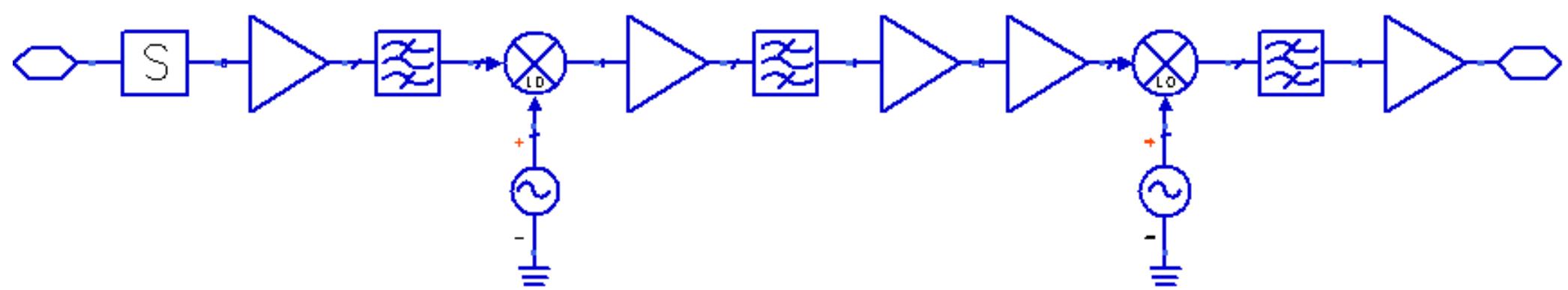
*system-level interactions*

- Top-level system brainstorming
- Quick analysis of circuit interactions
- Budget analysis to allocate circuit specifications
- Design partitioning



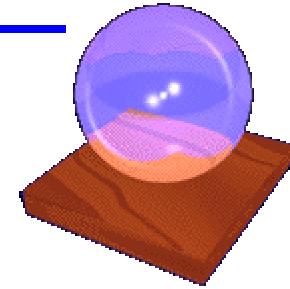
Quickly and accurately analyze system performance !

# Block & Level System Budget Analysis

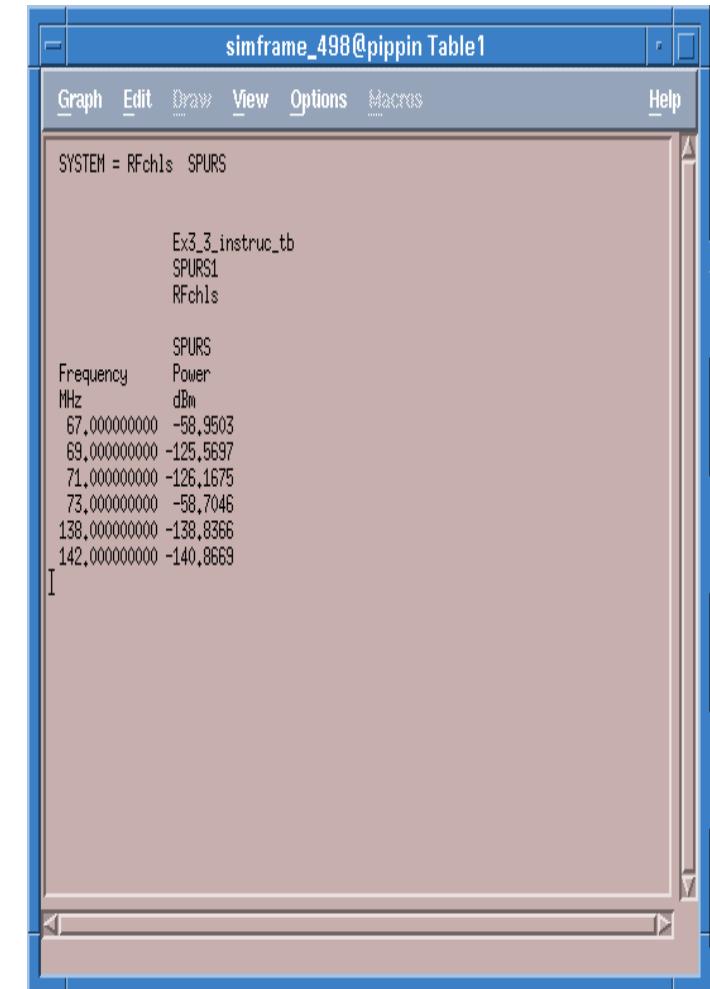
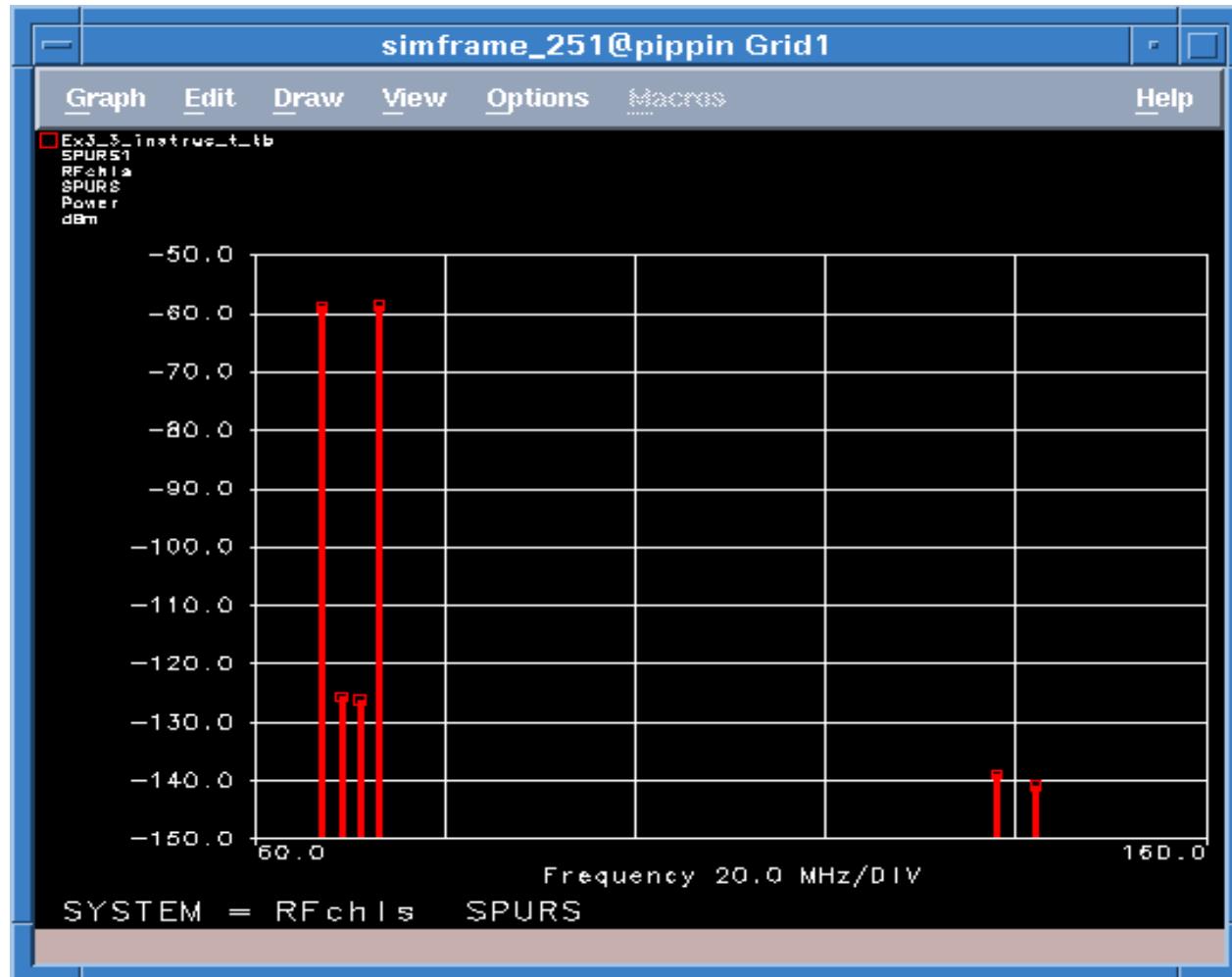


<b>Element</b>	<b>Duplexer</b>	<b>LNA</b>	<b>BPF</b>	<b>Mixer</b>	<b>AMP #1</b>	<b>BPF</b>	<b>AMP #2</b>	<b>AMP #3</b>	<b>Mixer</b>	<b>BPF</b>	<b>AMP</b>
<b>Gain (dB)</b>	-3	20	-2.7	-7	20	-17.4	30	30	-6	-6	45
<b>Noise Figure (dB)</b>	2.7	1.5	2.7	7.5	4	17.4	4	6	6	6	5
<b>NFO (dB)</b>	2.7	4.2	4.3	4.7	5.1	5.3	5.6	5.6	5.6	5.6	5.6
<b>Power (dBm)</b>	-125.3	-103.9	-107	-114.4	-94.1	-111.5	-81.5	-53.2	-58.9	-65	-19.9
<b>SNR (dB)</b>	6.5	4.9	4.9	4.5	4	3.9	3.6	3.6	3.6	3.6	3.6
<b>TOI @ Output (dBm)</b>		3.2	0.5	-7.5	8	-9.4	9.1	24.2	15.8	9.8	20

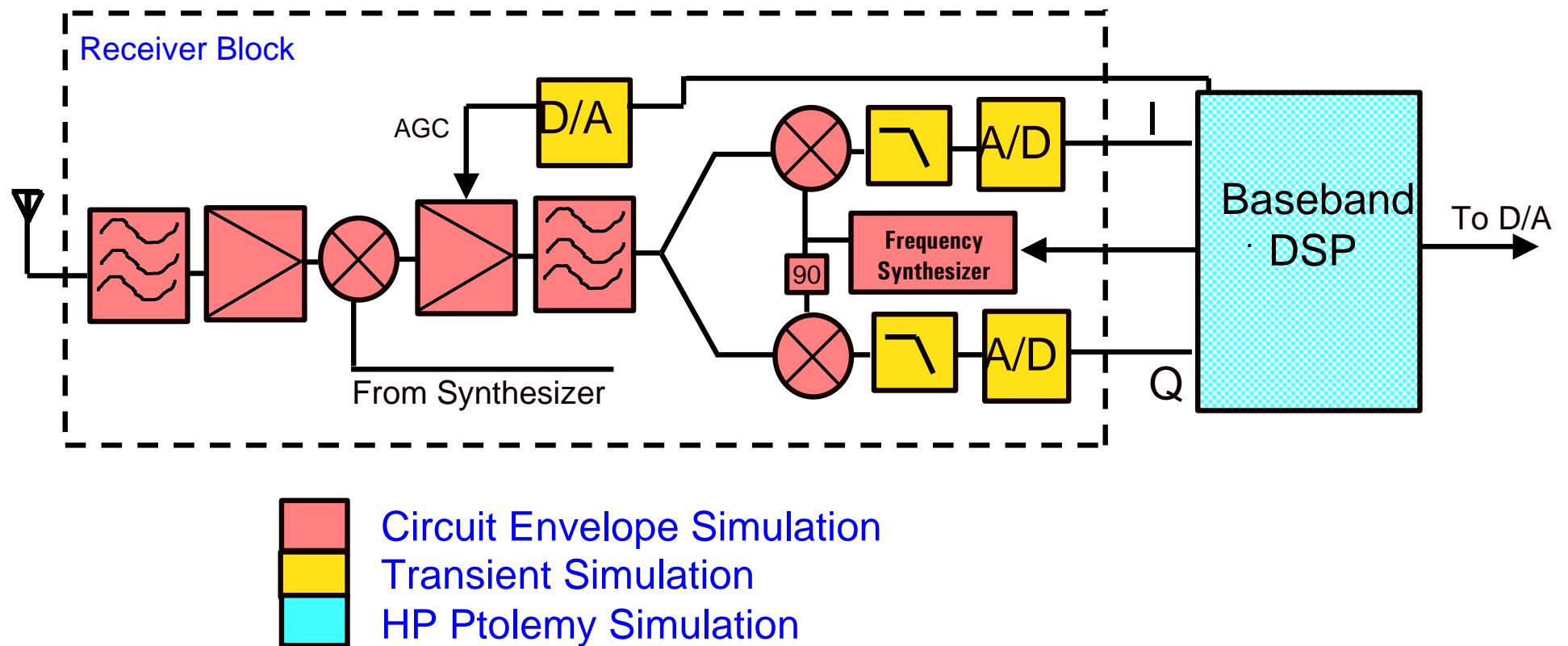
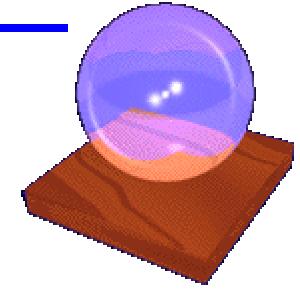
# Classic Example: Spur Analysis



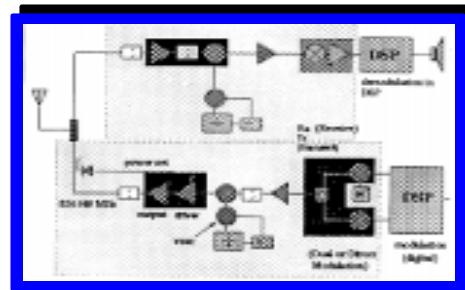
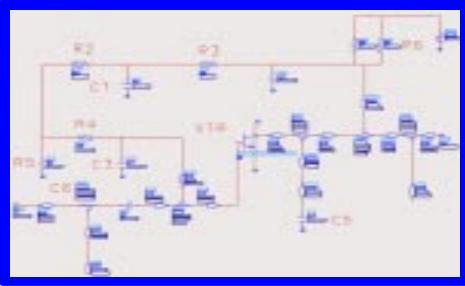
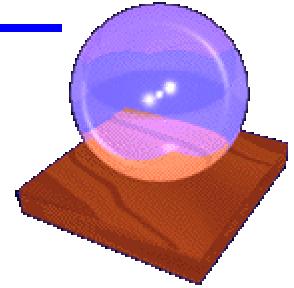
Select frequency plan based on predicted performance



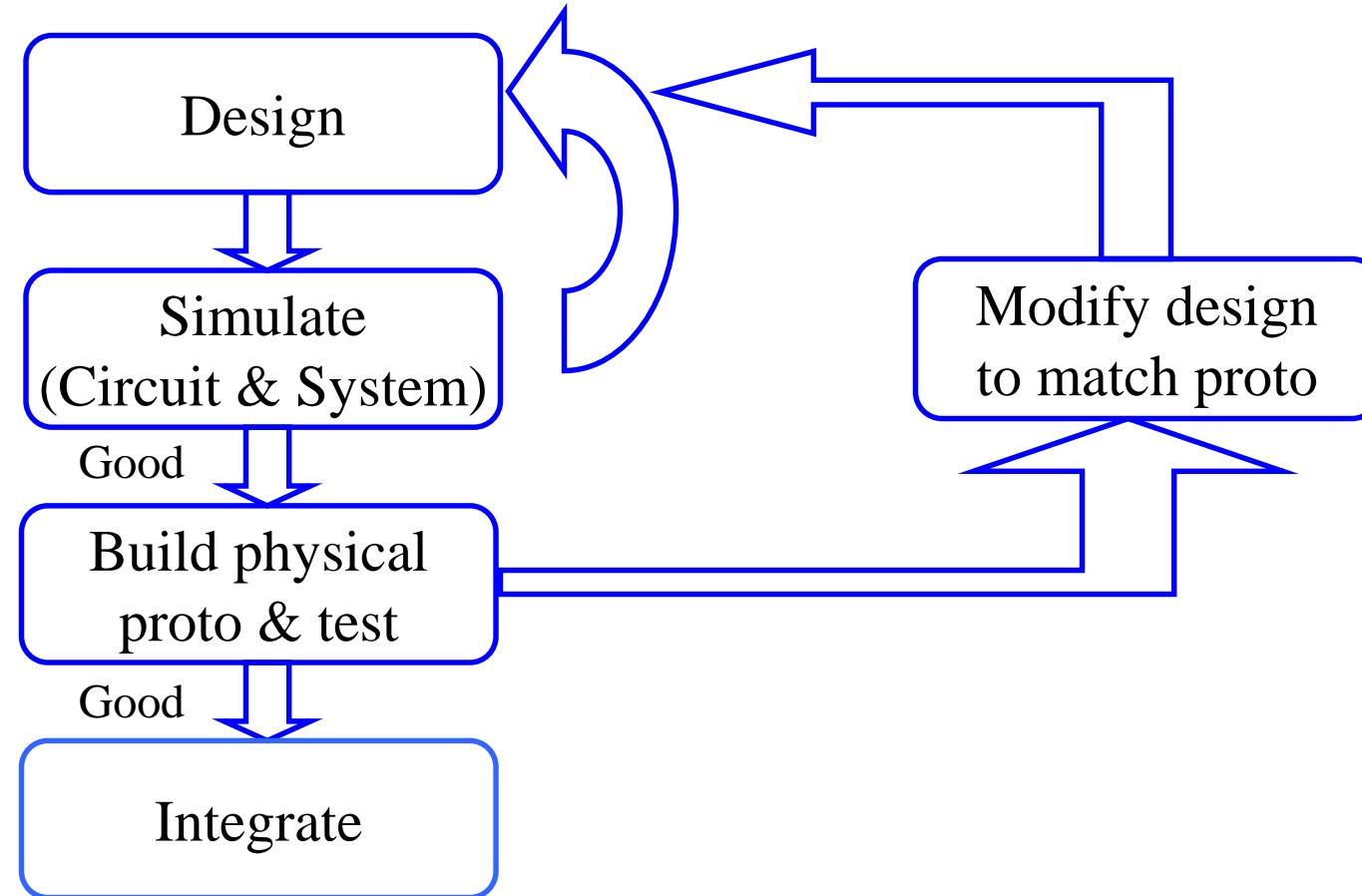
# Integrated Design Environment



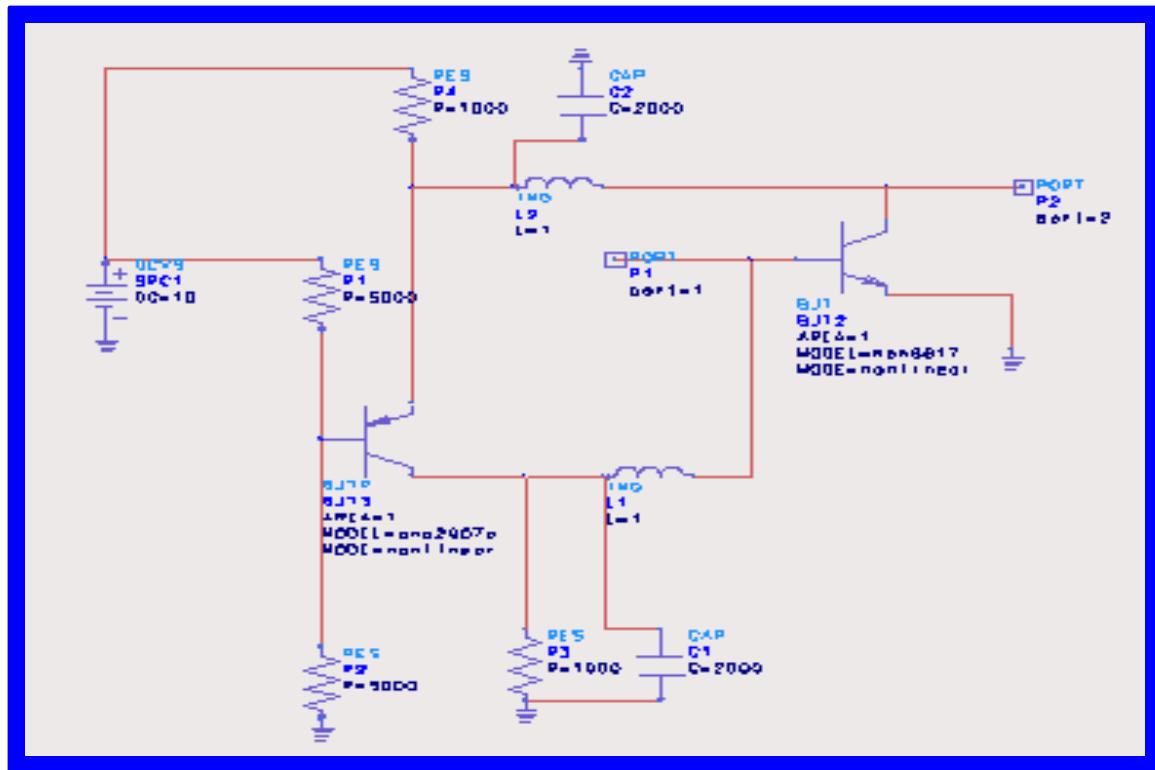
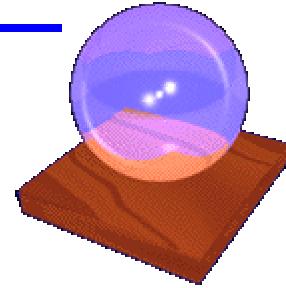
# Circuit Design Cycle



 HEWLETT®  
PACKARD



# Circuit Design Brainstorm



- Experiment with possible biasing schemes
- Explore different circuit configurations
- Make many different analyses quickly

# Why Modify Design to Match Prototype?



First, verify that there are no errors in the fabrication or measurement of the prototype.



Why modify the design to match the prototype?

- Provides starting point to refine design
- Gives good assurance that design changes will indeed improve design



The closer prototype matches the model, the greater the probability for success :

$$Ps = (k) \cdot x^c \cdot 100$$

where

***Ps = success probability***

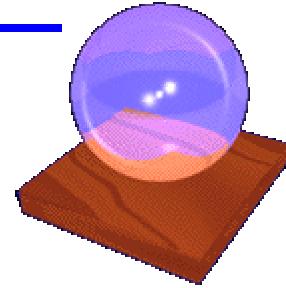
***c = # of changes***

***k = guru factor (<1.0)***

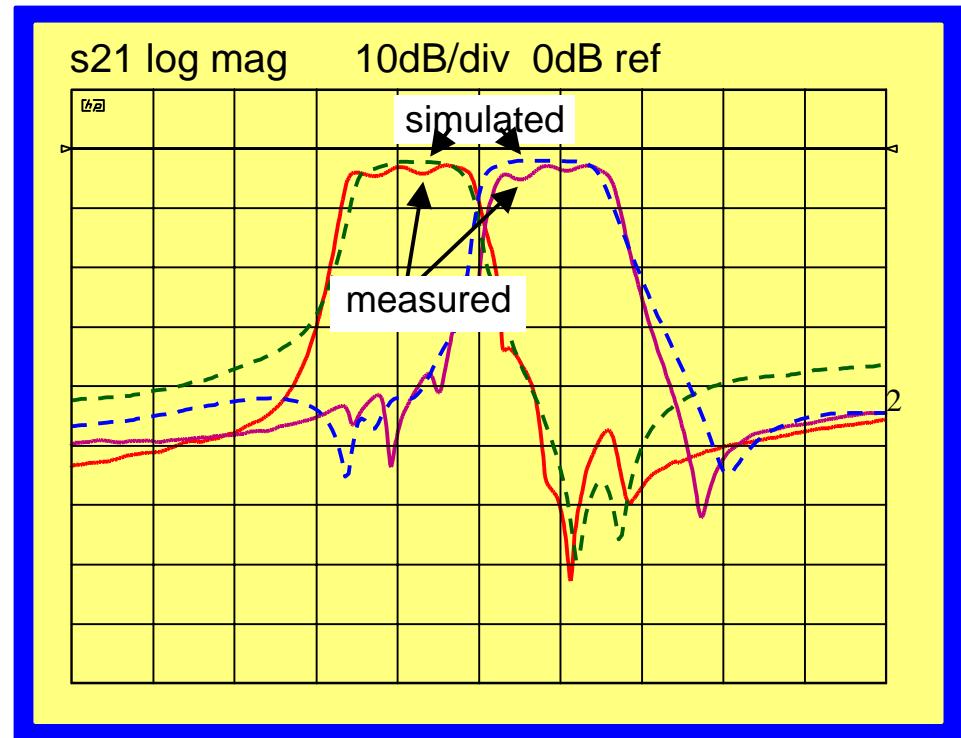
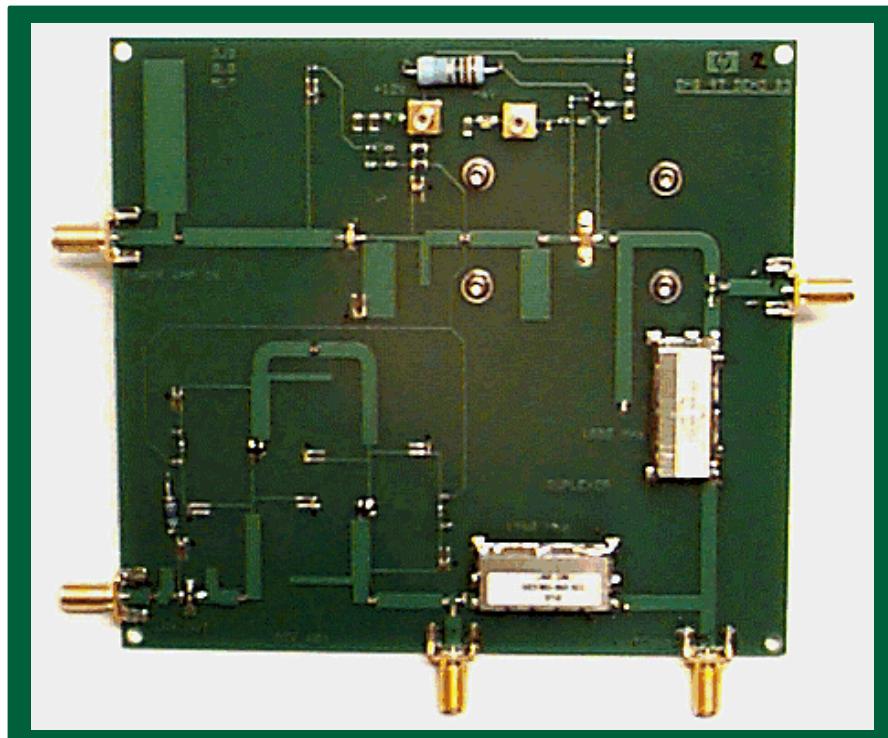
**Careful!  
Proceed with  
caution.**

*Continuing to  
optimize with-  
out a physical  
prototype*

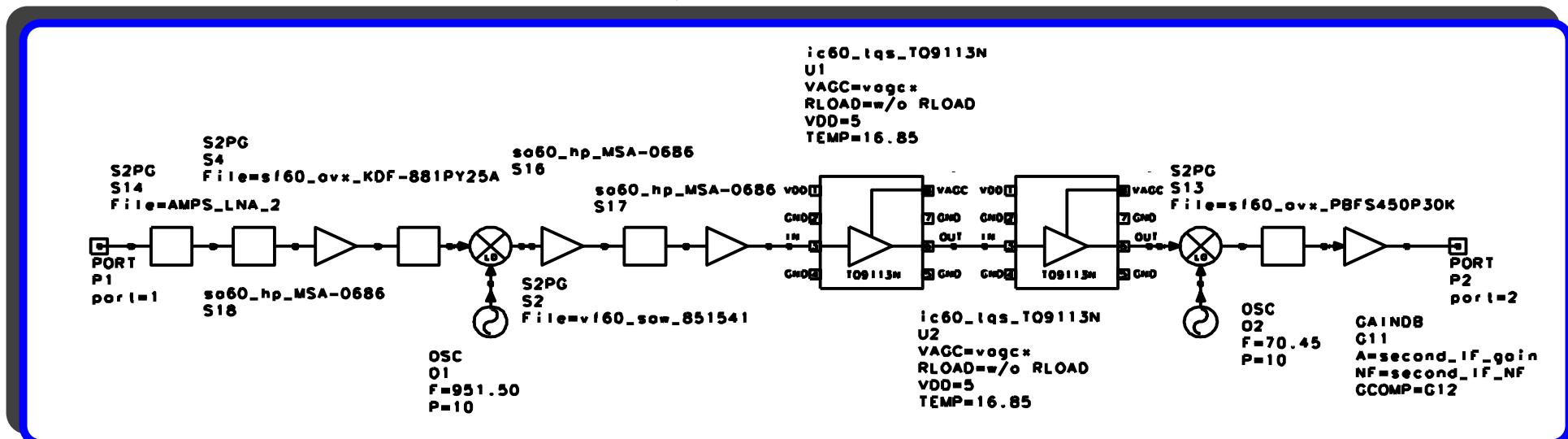
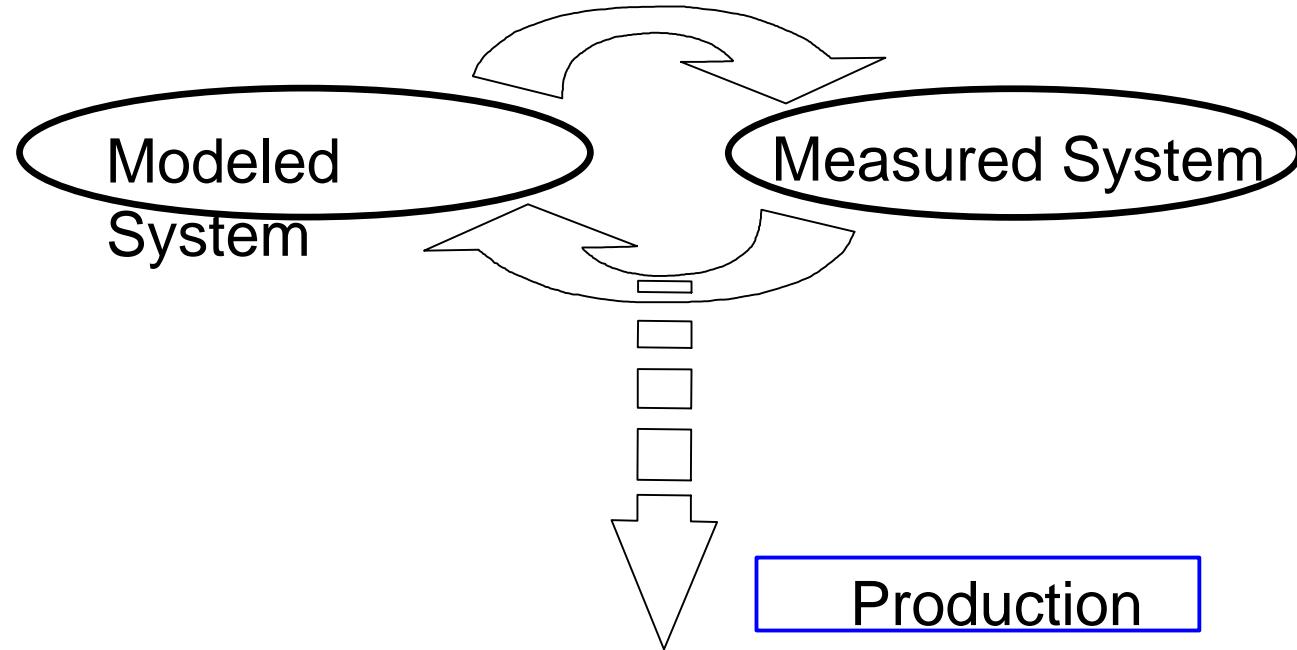
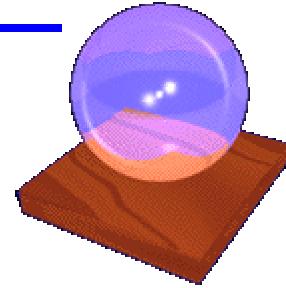
# Integration: Layout & Prototype



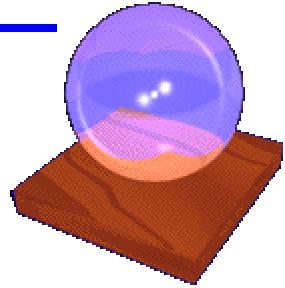
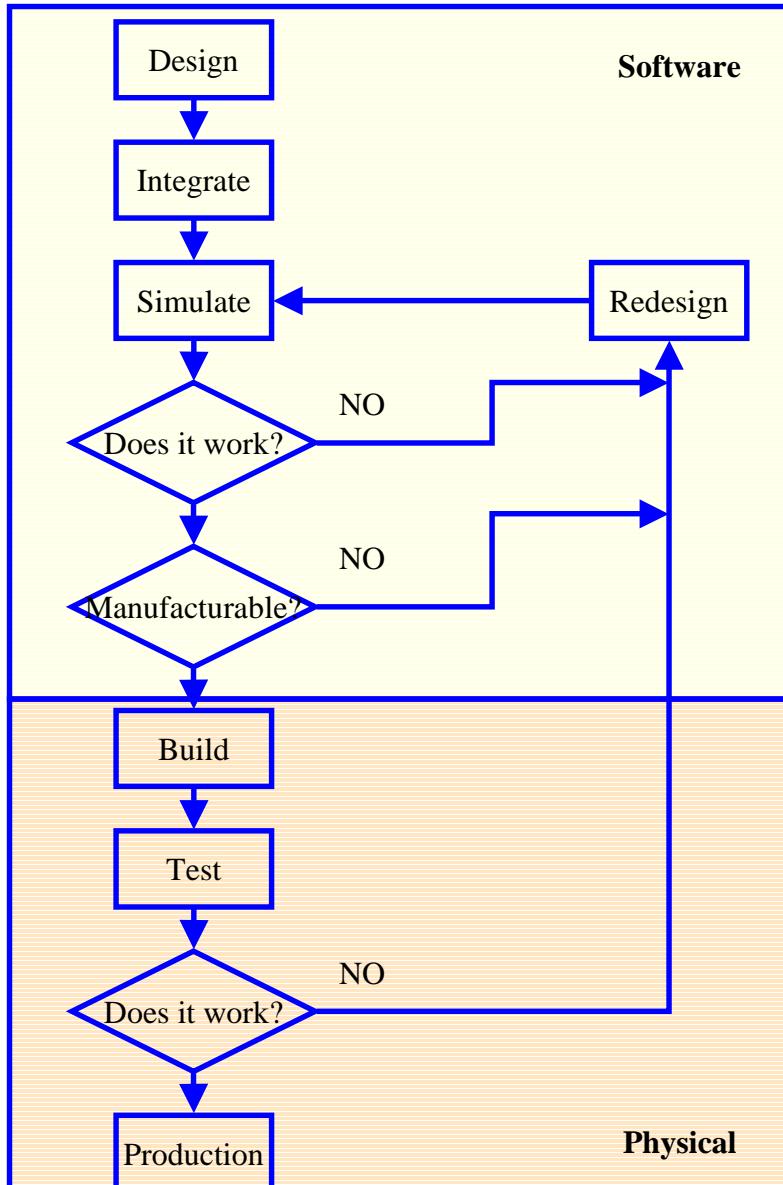
- Interconnect designs and measure performance
- Modify design to reflect measured results (if necessary)



Success!  
Measured = Modeled & Exceeds Spec

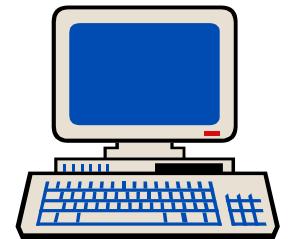


# The Predictive RF Design Process



Concept

Design



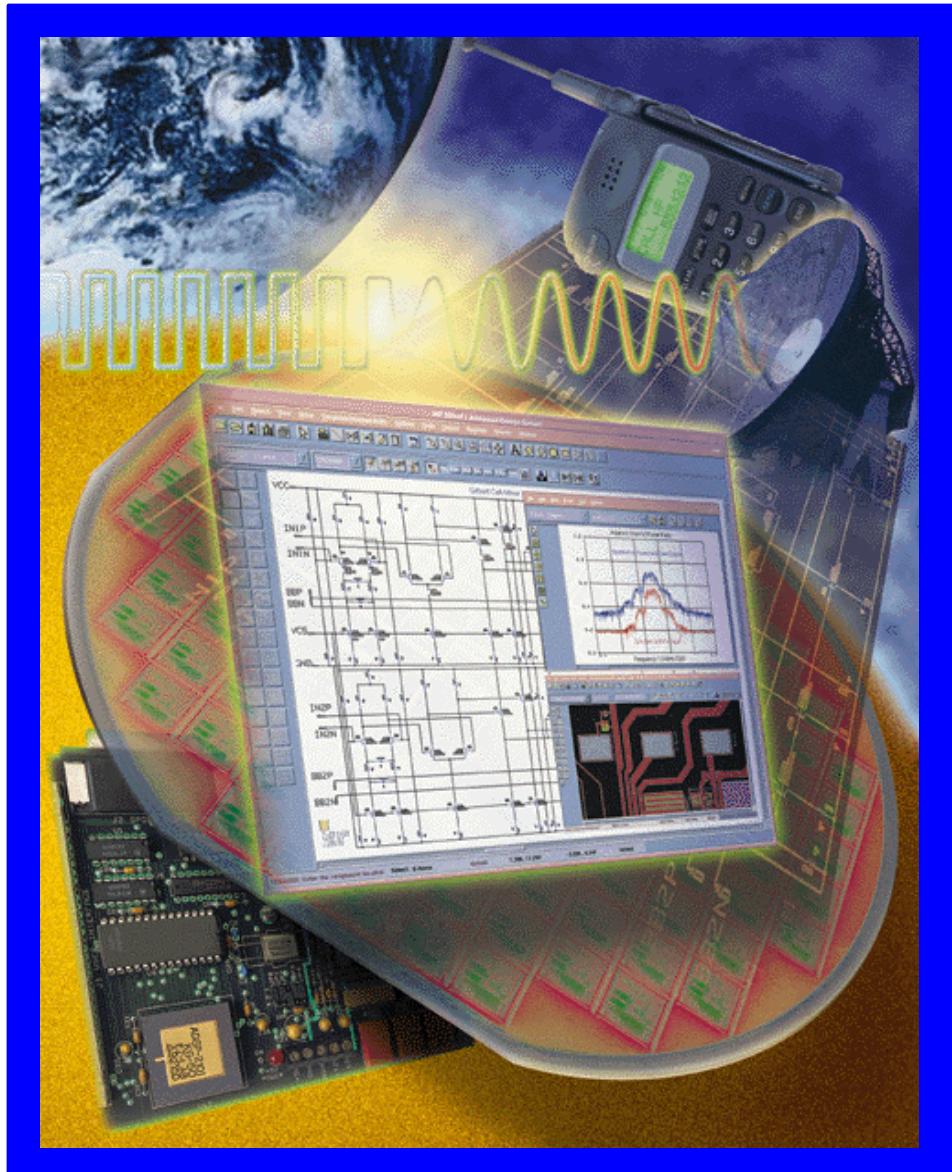
Integrate

Production

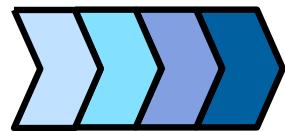


- Tweak the design on the work station, not on the bench!

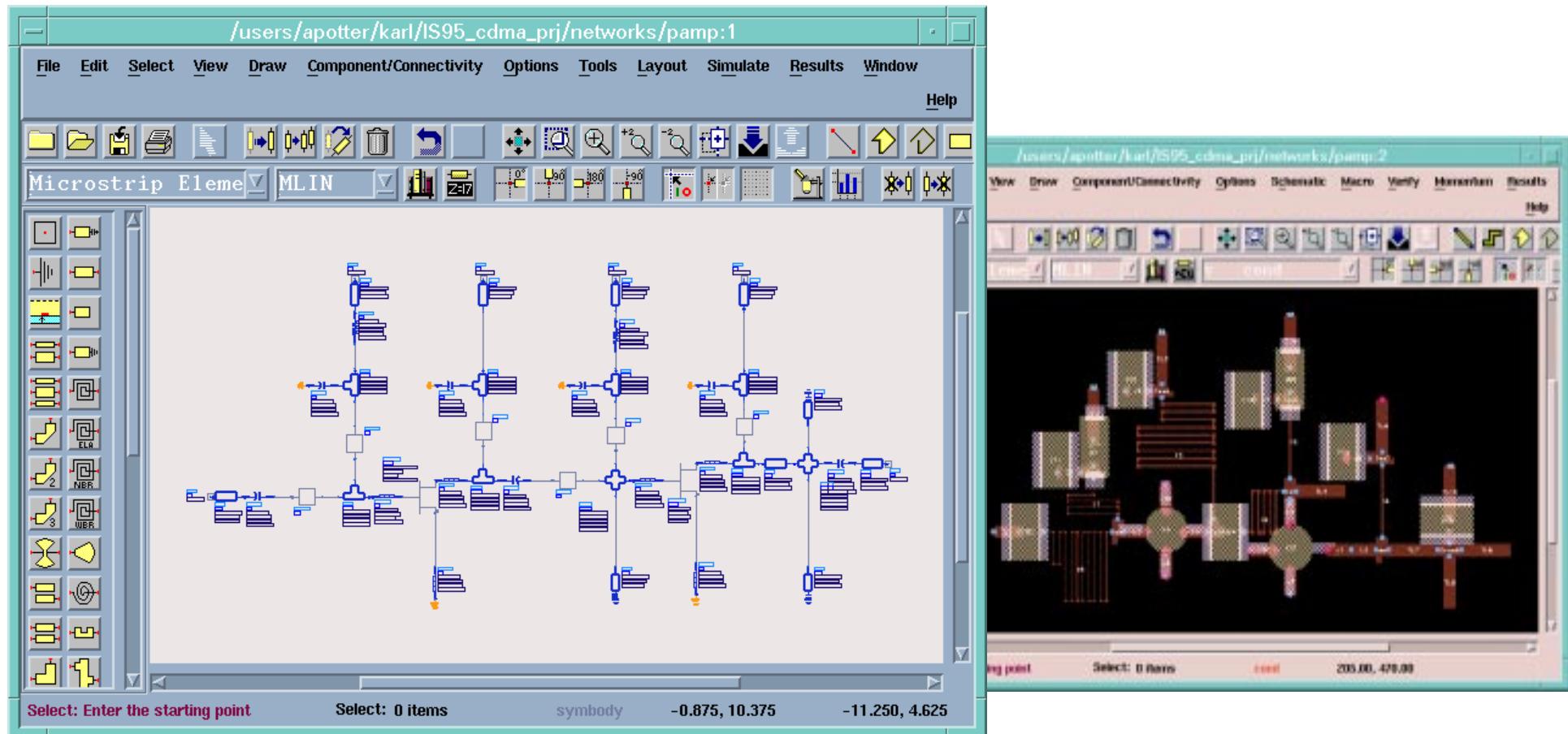
# Solutions from Hewlett-Packard



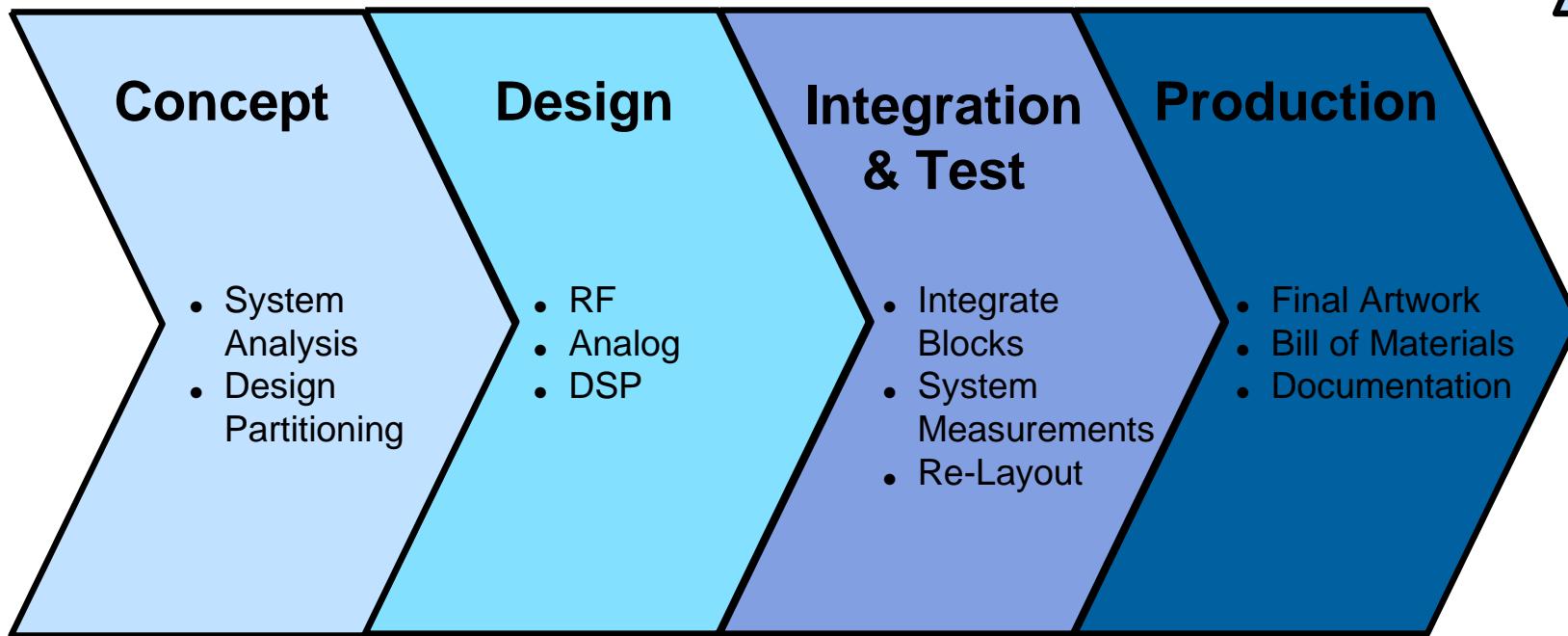
# HP Advanced Design System



Total integration of schematic, simulation, and layout



# The RF Design Process



- Co-Simulation
- System Simulation
- Integrated Simulators
- Faster Simulators
- Optimizers
- Instrument I/O
- Parts Libraries
- Layout
- EM Simulation
- Parts Libraries
- Third Party Links
- Artwork Generation

# HP's Measurement Instrumentation

- HP Advanced Design System
- Network and Signal Analyzers
- Protocol Signal Sources (CDMA, GSM, etc.)

