EL 351 - Linear Integrated Circuits Laboratory

Design and Test of Digital-to-Analog Converters

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Equipment:

- Agilent 54622A Deep-Memory Oscilloscope
- Agilent E3631A Triple-Output DC power supply
- Agilent 33120A Function Generator
- Agilent 34401A Digital Multimeter

Introduction:

A great deal of information is stored in digital form (music, pictures, oscilloscope traces), yet must be converted to, and "displayed" as, analog voltages. The conversion of digital information to an analog format (current or voltage) is done by a digital-to-analog converter, commonly known as a DAC.

Key specifications of a DAC include the number of bits of the digital input, and the range of the output current or voltage. For example, a DAC may have a 10 bit input word, and the output may range from 0 V to +5 V, or -5 V to +5 V.

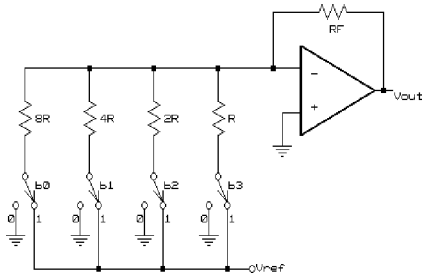
In this experiment you will design two different 4-bit DAC circuits, and test them over the full range of digital input word (0000 to 1111, in binary).

Procedure:

Design and Test of Weighted Summer DAC

1. Design a weighted summer DAC, such that $V_O = +(2/3)(8b_3 + 4b_2 + 2b_1 + b_0)$, where b_3 = MSB (the most significant bit b_3 is either 1 or 0, and represents $2^3 = 8$) and b_0 = LSB (the least significant bit b_0 is either 1 or 0, and represents $2^0 = 1$). Example: if the digital input is a binary 1011 (that's 1011_2), the output voltage would be $V_O = +(2/3)(8[1] + 4[0] + 2[1] + [1]) = +(2/3)(11) = 7.33$ V.

   See the weighted summer circuit below.



   Use supply voltages of +/- 15 V, use a 741 or LF 351 op-amp, and give consideration to two issues:

   a. the power dissipated by all resistors, and

b. standard values of should be used for all resistors (*which means your DAC will not have perfect linearity; this is OK, and will make an interesting graph*).

Draw a neat, professional looking schematic diagram of your circuit, and have your design approved by your instructor before proceeding. _____

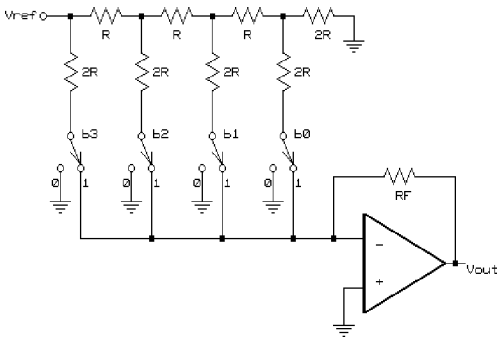
2. Construct the circuit, making it easy to change a given bit from a 1 to a 0. Jumper wires work well for this purpose.

3. Create a table of output voltage vs. input digital word, as the digital word varies from 0000_2 to 1111_2. Be sure to perform an offset null adjustment on your op-amp circuit before beginning, so that when the input is 0000_2, Vo = 0.00 V. The offset null can be accomplished by putting a 20k Ω potentiometer between pins 1 and 5 of your op-amp, connecting the wiper to the negative supply voltage, and adjusting the wiper until Vo = 0.00 V. Do **NOT** disconnect the negative supply from pin 4.

Design and Test of an R-2R Ladder DAC

1. Design an R-2R ladder DAC, such that $V_O = -(1.0)(8b_3 + 4b_2 + 2b_1 + b_0)$, where b_3 = MSB (the most significant bit b_3 is either 1 or 0, and represents $2^3 = 8$) and b_0 = LSB (the least significant bit b_0 is either 1 or 0, and represents $2^0 = 1$). Example: if the digital input is a binary 1101 (that's 1101_2), the output voltage would be $V_O = -(1.0)(8[1] + 4[1] + 2[0] + [1]) = -(1.0)(13) = -13$ V.

See the R-2 ladder circuit below.



Use appropriate supply voltages, use a 741 or LF 351 op-amp, and give consideration to two issues:

a. the power dissipated by all resistors, and

b. standard values of should be used for all resistors (*which means your DAC will not have perfect linearity; this is OK, and will make an interesting graph*).

Draw a neat, professional looking schematic diagram of your circuit, and have your design approved by your instructor before proceeding._____

2. Construct the circuit, making it easy to change a given bit from a 1 to a 0. Jumper wires work well for this purpose.

3. Create a table of output voltage vs. input digital word, as the digital word varies from 0000_2 to 1111_2. Be sure to perform an offset null adjustment on your op-amp circuit before beginning, so that when the input is 0000_2, Vo = 0.00 V. The offset null can be accomplished by putting a 20k Ω potentiometer between pins 1 and 5 of your op-amp, connecting the wiper to the negative supply voltage, and adjusting the wiper until Vo = 0.00 V.

Lab Report:

1. Create a graph of Vo vs. input word for your weighted summer DAC. On the same axes, plot the transfer characteristic for an ideal 4-bit DAC with the same output voltage range, but with perfect linearity. Comment on the differences between your DAC and the ideal DAC, including the magnitude of the errors.
2. Create a graph of Vo vs. input word for your R-2R ladder DAC. On the same axes, plot the transfer characteristic for an ideal 4-bit DAC with the same output voltage range, but with perfect linearity. Comment on the differences between your DAC and the ideal DAC, including the magnitude of the errors.
3. What are some significant problems associated with a weighted-summer DAC compared with an R-2R ladder DAC?