Syllabus: Digital Logic Design

By: Dr. A. D. Johnson
EECS: 1100 Digital Logic Design
The University of Toledo

Week	starting	Subject
1.	January 11	Ch.1 Number Systems and Codes. - (Emphasis on integers)
2.	January 18	Ch.2 Sections 2.1 through 2.3 Switching circuits.
3.	January 25	Ch.2 Sections 2.4 through 2.5 Synthesis of combinational circuits.
4.	Febr. 1	Ch.2 2.5 Synthesis of combinational circuits.
5.	Febr. 8	Ch.3 Sections 3.1 through 3.3 Karnaugh Map.
6.	Febr. 15	Ch.3 Sections 3.3 through 3.5 Simplification using K-Maps. `Quiz#1`
7.	Febr. 22	Ch.4 Sections 4.1 through 4.3 Encoders.
8.	March 1	Ch.4 Sections 4.4 through 4.7 Comparators.
9.	March 15	Ch.6 Sections 6.1 through 6.4 Flip-flops.
10.	March 22	Ch.7 Sections 7.1 through 7.3 Counters.
11.	March 29	Ch.7 Sections 7.3 through 7.5 Shift registers as Counters.
12.	April 5	Ch.8 Sections 8.1 through 8.3 Synchronous sequential circuit synthesis.
13.	April 12	Ch.8 Sections 8.3 through 8.4 Incompletely specified circuits.
14.	April 19	Ch.5 Combinational circuit design with programmable devices
15.	April 26	Ch. 11 Section 11.1 through 11.3 Sequential Circuit Design and PLD device selection.

Goals:	Gaining basic contemporary knowledge and skills in analysis and design of logic circuits.
Textbook:	V.P.Nelson, H.T.Nagle, et al.: Digital Logic Circuit Analysis &Design, Second Edition, Prentice Hall, 1995. ISBN 0-13-463894-8
Grading Policy:	Homeworks / Lab / Quiz #1 / Quiz #2/ Final exam =10 / 24 / 15 / 15 /36.
Homework grader:	Mr. John Kary, NI-2045, Mr. Donald Ondrejka, NI-2045, MWF 11:00-1:00 & 2:00-3:00 & TR 10:00-11:00 &12:20-2:00.

2. Lab Information

2.1 Lab Room: NE-1036 - Digital Logic Design Lab

2.2 SCHEDULE OF LAB HOURS

Course section	Time	TA	Office	Office hours
1100:001	T 2:00-4:20	Konstantin Muranov	NE-1035	WF 12-1.30PM
1100:002	R 2:00-4:20	Konstantin Muranov	NE-1035	WF 12-1.30PM
1100:003	W 12.00-2.20	Sabra Mahir	NE-1035	MW 11.-12.00PM
1100:004	M 3:00-5:20	Mona Saxena	NE-1035	W 3.00- 5.00PM
1100:005	W 3:00-5:20	Ram Padmanaban	NE-1035	W 3.00- 5.20PM
1100:006	F 2:00-4:20	Jandhyala Gopal	NE-1035	F 11.-1.00PM
1100:007	M 12.00-2.20	Sabra Mahir	NE-1035	MW 11.-12.00PM
1100:008	R 11:00-1:20	Sabra Mahir	NE-1035	MW 11.-12.00PM

* Telephone # in NE-1035: 530-8287.

2.3 SCHEDULE OF LAB ASSIGNMENTS

Lab sessions start the very first week of the semester. The full text of the Lab Assignment #1 has already been posted, and all further Lab Assignments will be posted at the EECS1100 web site:

http://www.eecs.utoledo.edu/Course_Information/EECS1100/EECS1100.html

Lab teams are responsible for downloading their Lab Assignment texts. The *Prelab Assignment* section of a Lab Assignment prepares students for experimental work in the Lab. Presentation of the computer generated results of the Prelab Assignment to the TA at the beginning of a Lab session is a prerequisite for the experimental work (this prerequisite will be waved for the sections which meet on Monday, January 11, 1999).

Digital Logic Design Lab has been recently equipped with state of the art instruments, whose sophistication provides opportunity for enriching the contents of Lab experiments at no additional cost in time. To take advantage of this opportunity, a major redesign of experiments has been initiated in the 1998 Fall Semester, and will be continued during the Spring Semester of 1999. The redesign being labor intensive, we reserve the right of minor last day updates outside the Prelab Assignment Section, although every effort will be made to have the text up on the web one week in advance. The set of Fall Semester Assignments has been left posted and will be updated as time progresses. Please, have a look at the *Spring 1998 Lab Handouts* to gain a full insight into the extent of changes which are taking place. Your understanding and cooperation will be greatly appreciated. Your learning experience will be rewarding.

3. Homeworks

3.1 PROBLEM SET OVERVIEW

Set#	Problem set contents	Selection	Semester week due
#1	1.4, *1.5*, 1.6, 1.7, 1.8, 1.9, 1.10, 1.12, *1.13*(BCD), 1.14, 1.15, 1.18.	all	2
#2	*2.1*, 2.2, 2.6, 2.7, 2.8, 2.12, *2.13*, 2.14, 2.16, 2.17,	(a) and (c)	3
#3	2.18, 2.19, *2.20*, 2.21,2.23, 2.24, 2.25,	(a) and (c)	4
#4	*2.28*, 2.30, *2.31*, 2.33, 2.34, 2.35, 2.36	(a) and (c)	5
#5	3.2(a,c), *3.3(a,b)*, 3.6(a), 3.16, 3.20, 3.22, 3.25, *3.30(b)*, 3.32, 3.35, 3.41, 3.44(b), 3.46(b), *3.50*, 3.53(a),	all	7
#6	4.1, 4.3, 4.4(b), 4.5, 4.11, 4.15, 4.18(a,b),) 4.19(a,b), 4.21, 4.33, 4.35, 4.40	all	9
#7	6.4, 6.6, 6.9, 6.14, 6.15, 6.17, 6.19	all	10
#8	7.3, 7.6, 7.9, 7.11	all	13
#9	8.1(a,b). 8.2(b,c), 8.3(b,c), 8.8, 8.10, 8.11, 8.13(b,c), 8.17, 8.24, 8.27	all	14
#10	5.1(a,b,d), 5.2(b,c,d), 5.3	all	15
#11			
#12			

3.1 POLICY ON SUBMISSION OF HOMEWORKS

1. All homework reports (solutions) are due at the beginning of the **second class of the week.**
2. In order to discourage the practice of working to finish the reports during the time scheduled for classes, the absolute deadline for handing in the reports is five minutes after the time scheduled for the beginning of the class.
3. Homeworks handed in after the deadline, but before the beginning of the first class of the next week are accepted for half credit.
4. This policy promotes good planning habits. The fact that something went wrong the morning of the due day does not make a case for delaying the due time. We ought to be prepared for the day when something unforeseen happens.